

Spherical Silicon Photovoltaics:
Material Characterization and Novel Device Structure

by

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Author's Declaration

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners.

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Abstract

Single crystalline silicon spheres have been used as alternative material for solar cell fabrication. This innovative technology has several advantages over traditional wafer technology. However, the material, process flow and characterization techniques are very different from the planar technology due to the spherical geometry. In material characterization, microwave photoconductivity decay is used to measure carrier lifetime. This technique is analyzed theoretically by mathematical treatment in this thesis. Furthermore, the carrier lifetime is measured in order to investigate rapid thermal grown oxide quality in the role of surface passivation of silicon sphere.

A traditional way of making spherical cells is to create a p-n junction by high temperature diffusion of phosphorous dopants into p-type silicon spheres. To further reduce the fabrication cost, a low temperature epitaxial film highly doped with phosphorous is deposited on the sphere surface to form an emitter layer using Plasma Enhanced Chemical Vapour Deposition (PECVD). The process flow of device fabrication is very different from silicon wafer thus a new set of process steps are derived for silicon spheres. Two main device structures, omission of insulating layer and silicon nitride as insulating layer between emitter film and substrate, are proposed. The deposition parameters, pressure, power, and deposition time are optimized for spherical geometry. The quality of the junction is evaluated by its current-voltage characteristic and capacitance-voltage characteristic. The results are also compared to similar device structures in planar technology. To examine the photovoltaic performance, illuminated current-voltage measurement is taken to provide information on short circuit current, open circuit voltage and fill factor. Furthermore, spectral response of quantum efficiency is investigated to assess the ability of carrier collection for a spectrum of wavelength. Limitations on spherical diode performance are concluded from the measurement results.

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Chapter 1

Introduction

In recent years, lots of innovations and developments have taken place in the photovoltaic industry. As conventional energy production is getting more expensive and people start to recognize alternative energy, solar power is anticipated to be the main energy production resource in the future [1]. In order to realize the optimistic prediction, the manufacturing cost of solar cell has to be brought down to a level which is comparable to the other energy production costs. The first generation silicon wafer solar cells have been commercially realized but the module installation cost is fairly expensive [2]. Currently massive efforts have been invested in thin film technology. This innovation has greatly reduced the material cost. In this thesis, a potential solar cell technology, spherical silicon solar cell, is investigated.

1.1 Introduction on Photovoltaics

Photovoltaic energy conversion involves conversion of light energy to electrical energy with the use of light absorbing material. Crystalline silicon, being the first material used as photovoltaic energy conversion, is still the dominant technology in today's market with more than 90% market share [3]. Single crystalline silicon gives exceptional performance on efficiency and stability but its manufacturing process is complicated and expensive. For applications with less stringent efficiency requirement, polycrystalline silicon is used for the economical reason. Other crystalline silicon fabrication techniques such as ribbon silicon and silicon film have been developed throughout the photovoltaic history to minimize fabrication cost. Another form of silicon without crystalline structure known as amorphous silicon opens a new area of research in silicon technology. Instead of high temperature growth as in crystalline silicon, amorphous silicon only requires low temperature deposition which greatly reduces the thermal budget. Although the efficiency of amorphous silicon is significantly lower than that of crystalline silicon

and amorphous silicon experiences light induced degradation over the lifetime of operation, the reduction in material use and its inherent flexibility make this option very suitable for low-cost flexible applications. In addition to silicon technology, other semiconductor compounds are proven to exhibit remarkable performance. Some of the common semiconductor compounds are gallium arsenide (GaAs), copper indium gallium selenide (CIGS) and cadmium telluride (CdTe). Nonetheless, silicon technology has a long history in photovoltaic, and it will still have a significant contribution in the future photovoltaic market.

1.2 Motivation for Research

The use of spherical silicon for manufacturing photovoltaic device is driven by low material cost and high throughput fabrication process. This research has been focused on simplifying the fabrication process and reducing the processing costs. In traditional spherical diode fabrication, the emitter layer is formed by high temperature diffusion. In order to save on thermal budget, the temperature of emitter formation can be lowered by using Plasma Enhanced Chemical Vapour Deposition (PECVD). The deposited junction technique has been thoroughly studied on planar single crystalline and multicrystalline silicon substrate and the results are promising. Another advantage of deposited junction is that it can eliminate the step of thinning down the emitter layer. In summary, it is worthwhile to invest effort in low temperature deposited junction on spherical silicon. The research, however, experiences a number of challenges due to the special geometry. Many contemporary processing techniques are tailored for planar technology thus a new set of process flow has to be designed to accommodate non-planar surface. The purpose of this research work is to address the complexity and derive techniques to fabricate the novel device.

1.3 Thesis Organization

This thesis contains seven chapters to explore the topic. Chapter 2 provides some background information on spherical silicon technology and also thin film deposition technology. Chapter 3

addresses the issues of carrier lifetime characterization. A theoretical treatment was conducted on carrier lifetime measurement and this measurement technique is applied to investigate the effect of rapid thermal oxide passivation of spherical silicon. Chapter 4 focuses on the development of a novel technology specifically designed for spherical silicon. The differences between planar and spherical geometry are investigated in terms of currently available processing techniques. Based on the differences, a new process flow is derived. Furthermore, two ways of providing insulating layer in spherical cell are proposed and evaluated. Chapter 5 encapsulates the experimental results of low temperature deposited junction and examines the junction quality. The deposited films with different deposition parameters are experimented on in order to optimize the film for spherical surface. Both current-voltage characteristic and capacitance-voltage characteristic are employed to evaluate the junction quality and compare with the planar diode. Chapter 6 attempts to look at the novel diode functioning as a photovoltaic device. The illuminated current-voltage characteristic and spectral response are thoroughly discussed. Analysis is performed to investigate why spherical photovoltaic does not achieve similar performance compared to planar photovoltaic. Chapter 7 summarizes the discussions throughout the thesis and comments on the outlook of spherical devices.

Chapter 2

Review of Spherical Silicon and Thin Film Deposition Technology

The use of spherical silicon as solar cell was first demonstrated in 1959 [4]. The special geometry gives rise to advantages such as high rate of crystal growth, robust mechanical properties, and flexibility in module design. In the years of development, the fabrication process of spherical silicon has been refined to lower the cost and increase the production rate. In order to accommodate the special geometry, a commercial process has been invented to account for the new material. This process, to be discussed in section 2.1, was developed by Texas Instruments in the 80s known as Spherical SolarTM Technology (SSP) [5]. In parallel, silicon thin film technology has undergone rapid development in recent years. It is of great interest to combine these two novel technologies to produce a functional photovoltaic device.

2.1 Spherical Silicon Fabrication

Spherical solar cell is made of large number of single crystalline silicon balls with a small diameter of around 1 mm, although smaller size spheres as small as 0.4 mm in diameters have been used [5]. A scanning electron microscope image of spherical silicon is found in Figure 2.1. Ideally spherical silicon possesses single crystalline quality as silicon wafer, but its production cost is greatly reduced due to alternative fabrication process. In addition to economic advantage, its final module matrix can exhibit flexibility if the substrate is made of flexible material such as aluminum foil. The motivation behind the research on silicon spheres is to fabricate low-cost silicon solar cell and achieve reasonable efficiency.

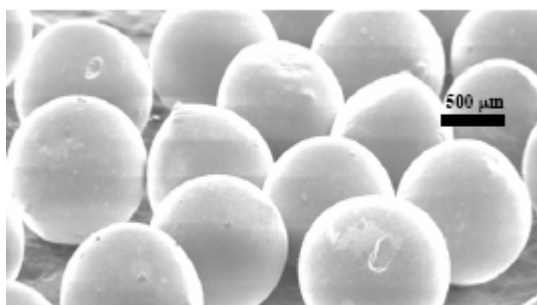


Figure 2.1. Scanning electron microscope image of silicon spheres

First of all, the feedstocks for spherical photovoltaic are very different from its planar counterpart. In order to grow wafer, a series of purification steps must be carried out on the metallurgical grade silicon until the impurity content reaches an acceptable level, which constitutes a large part in fabrication cost and time. Single crystalline growth begins with semiconductor grade silicon which requires sophisticated purification process. For spherical silicon, the materials for processing can come from a variety of sources [5]. In early development, upgraded metallurgical grade silicon was used as starting material for single crystalline growth. Later on, the use of off-spec semiconductor grade silicon, rod ends from Siemens process, kerf loss from wafer cutting, reactor dust, and undersize spheres were developed. The abundance of silicon feedstock results in a lower material cost for spherical photovoltaic. Also the high cost of separate purification process can be eliminated as the impurity removal process can be carried out in-situ with crystal growth.

The first step in crystal growth is the melting of the silicon feedstocks of various forms of irregular shape and size in a furnace in the process known as powder fusion [5]. In the same process, liquid boron dopants are added to dope the silicon. Because of the application of high temperature, dopants are distributed throughout the molten silicon. Afterwards, the polycrystalline product is converted to single crystalline spheres through a series of melting and removal/etching cycles. During controlled cooling, silicon crystallizes in spherical shape by surface tension and the impurities are segregated toward the surface where an oxide has been formed [6]. The impure

outer layer of the spheres can be removed by mechanical grinding or chemical etching with acid [7]. If the starting feedstock has a high level of impurities, the melting and removal/etching steps can be executed repeatedly to reduce the impurity level. For high quality off-spec semiconductor grade silicon feedstock, further melting is not required for impurity removal and a chemical etch can be performed to remove the oxide layer at the surface.

Further processing steps are necessary to prepare the sphere for cell processing. First a chemical polishing step is performed to provide the sphere with a mirror surface [5]. To further improve the bulk quality of the sphere, the impurities should be deactivated, which can be achieved by oxygen denuding. At a high temperature annealing of 1200 °C, oxygen contents within a few diffusion lengths below the surface diffuse out of the sphere. During the cooling, the remaining oxygen at the core precipitates to getter the metal impurities in the bulk. Finally, a chemical etch is carried out to remove the oxide.

2.2 Traditional Spherical Technology

To create a diode, a p-n junction must be formed. Derived from planar technology, phosphorous diffusion is used traditionally to form an n-type layer [8]. A diode is then constructed with the spherical p-n junction. The process is described below with pictorial schematic in Figure 2.2.

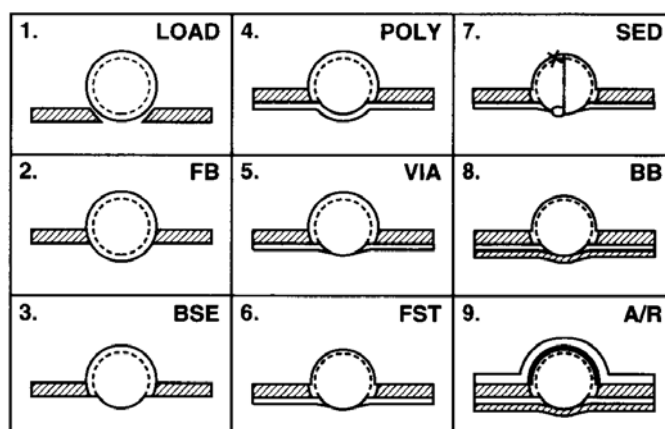


Figure 2.2. Cell processing in spherical technology [8]

In Spherical Solar Process, spheres are bonded to aluminum foil perforated with predefined hole size and hole-to-hole spacing by appropriate temperature and pressure [5]. The foil, also known as front foil, serves as the contact to the n⁺ layer. The bonding process has to be well controlled so the aluminum spikes do not penetrate into the p-type bulk. Then the backside of the spheres are subjected to a chemical etch removing n⁺ layer and allowing the p-type bulk to expose. To contact the p-type sphere, an insulating layer must be applied to separate the front and the back foil. A thin layer of polyimide is sprayed on the backside of the front foil as insulation. The film is then cured and mechanical abrasion selectively opens holes in the polyimide layer to expose the sphere bulk. To improve the short circuit current, a thinner emitter layer is desired. For thermal diffusion of phosphorus dopants, the emitter depth can extend to 1 μm below the sphere surface. Thus, a Front Side Thin (FST) process is conducted at the sphere surface to etch away the n⁺ layer to certain extends. For a large number of spheres connected in parallel to deliver power, defective spheres can create shunt paths which completely short the whole strip of spheres. Therefore, a technique called Selective Electro-Dissolution (SED) was invented in SSP to isolate the defective spheres. This process forms an insulating layer on the defective spheres separating them from the grid. Finally, a back foil can be applied to the back of the cells to create a contact with the p-type bulk by thermomechanical bonding. Antireflective coating such as titanium dioxide (TiO_2) is then applied to the front side of the spheres using atmospheric pressure chemical vapour deposition.

2.3 Low Temperature Thin Film Deposition

In Complementary Metal Oxide Semiconductor (CMOS) technology, the devices are fabricated only the first few microns at the surface. To ensure exceptional performance, the layer where the devices are active is made by epitaxial deposition. The epitaxial deposition is a thermal Chemical Vapour Deposition (CVD) process carried out at above 1000°C for crystalline silicon growth [9]. In CVD, the precursor gases, usually silane (SiH_4) and dopant gas, flow into the chamber. At sufficiently high temperature, the gases dissociate into radicals and diffuse to the substrate surface.

The radicals adsorb at the surface have enough energy to move around, find an energy favourable site and form a strong bond, resulting in a crystalline silicon growth with the same crystal orientation as the substrate.

If the temperature is lower, it is observed that the structure of the film changes from crystalline to polycrystalline. A further reduction of deposition temperature to about 450 °C results in amorphous silicon growth, which no orderly structures are found in the film. However, the thermal requirement in cracking precursor gases does not allow deposition to occur at low temperature. Plasma Enhanced Chemical Vapour Deposition (PECVD) addresses this problem. The plasma assists the dissociation of reactant gases by high-energy electrons bombardment. The dissociation process can occur at lower temperature of about 250°C and it is even possible to have thin deposition at room temperature. The PECVD system used in this thesis operates at a radio frequency of 13.56 MHz.

Recently, it is reported that PECVD can be used to deposit film with small crystals embedded in amorphous matrix. These films are known as microcrystalline and nanocrystalline depending on the size of the crystals [10 – 12]. By adding hydrogen to the chamber, the silane gas concentration is diluted resulting in slower deposition rate. On the other hand, hydrogen helps to etch the weak bonds during film growth and thus strong silicon-silicon bonds are more likely to form. The film to be investigated in this thesis, low temperature epitaxial film, also known as quasi-epitaxial film, built on this theory to mimic crystalline growth at low temperature.

Chapter 3

Material Characterization of Spherical Silicon

The starting material of spherical silicon processing is significantly different from that of planar silicon wafer; therefore, characterization of spherical silicon should be carried out to monitor the material quality. The material quality is directly related to the bulk quality, which impacts the device performance. In photovoltaic application, a high quality bulk can allow photogenerated carriers to successfully diffuse to the junction where they can be swept across. For this reason, carrier lifetime is an important parameter in material characterization for photovoltaic devices. Microwave photoconductivity decay is a contactless measurement technique which reduces the carrier lifetime. This technique can be made compatible with silicon spheres thus it will be the main tool to evaluate carrier lifetime.

3.1 Carrier Lifetime and Recombination Mechanisms in Silicon

In solar cell application, it is important to identify the minority carrier lifetime. When the cell is illuminated, photogenerated electron hole pairs are created in the bulk and excess minority carriers diffuse to the space charge region to be swept across and become majority carriers. In the diffusion process, the minority carriers may encounter defects which act as traps and cause the trapped carriers to recombine. By monitoring the carrier lifetime, it is possible to estimate the probability that the generated carriers reach the contact.

The carrier lifetime is limited by the recombination happening in the diode. There are three major recombination mechanisms contribute to the overall lifetime in semiconductor, Shockley-Read-Hall recombination, radiative recombination and Auger recombination as indicated in Equation (3.1) [13]. The symbol τ in (3.1) represents the minority carrier lifetime. Since silicon is an indirect bandgap semiconductor, radiative recombination can be safely discarded

in the following discussion because τ_{rad} can be assumed to be infinitely large compared to the other two contributions.

$$\frac{1}{\tau_{bulk}} = \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} \quad (3.1)$$

Shockley-Read-Hall (SRH) recombination is the dominant recombination mechanism in silicon. Since silicon is an indirect bandgap semiconductor, a successful electron hole recombination must be accompanied by a change in momentum, which can be accomplished by phonon emission, phonon absorption, or deep level traps located in the middle of the bandgap acting as recombination centers. Deep energy levels in the midgap are the result of impurities and defects in the silicon lattice. In SRH, energy level of carrier traps is modeled as an energy level located at the midgap. Although in reality there should be a spectrum of energy levels exist inside the bandgap, the carrier lifetime is approximated by a single energy level pinned at the midgap [13].

$$\tau_{SRH} = \frac{\tau_{p0}(n_0 + n_1 + \Delta n) + \tau_{n0}(p_0 + p_1 + \Delta p)}{(n_0 + p_0 + \Delta n)} \quad (3.2)$$

$$\tau_{p0} = \frac{1}{\sigma_p v_{th} N_T}, \tau_{n0} = \frac{1}{\sigma_n v_{th} N_T} \quad (3.3)$$

where n_0 and p_0 are the equilibrium carrier concentration, n_1 and p_1 are the carrier concentration at the trap energy level E_T , and Δn and Δp are the excess minority carrier concentration for electrons and holes respectively. The electron and hole lifetime τ_{n0} and τ_{p0} are inversely proportional to capture cross section σ , thermal velocity v_{th} and trap density N_T .

Auger recombination is prevalent in heavily doped semiconductor or when the semiconductor is subjected to high level injection. In low level injection, Auger recombination still takes place but its effect is insignificant since SRH recombination dominates.

In Auger recombination, an electron recombines with a hole and the energy released from recombination is absorbed by a third carrier. Because of the electron-electron-hole interaction or

electron-hole-hole interaction, the recombination rate is proportional to n^2p and np^2 respectively for three-particle participation, where n and p are the electron and hole concentration [14]. The ideal expression for Auger lifetime is expressed as [15]

$$\tau_{Auger} = \frac{1}{C_p(p_0^2 + 2p_0\Delta n + \Delta n^2) + C_n(n_0^2 + 2n_0\Delta n + \Delta n^2)} \quad (3.4)$$

where n_0 and p_0 are the equilibrium carrier concentration, Δn and Δp are the excess minority carrier concentration, and C_n and C_p are the Auger coefficients for electrons and holes.

Because Auger recombination is the dominant recombination in heavily doped region, n+ emitter layer which is usually highly doped with $10^{19}/\text{cm}^3$ mainly suffers from this recombination mechanism. In the p-type silicon bulk, Auger recombination mechanism has a lesser effect thus Shockley-Read-Hall recombination is assumed.

In addition to bulk recombination, surface recombination plays a significant role in carrier lifetime. The surface presents more pathways for carriers to recombine. At the surface where the silicon bonds are abruptly terminated, the dangling bonds can easily trap the approaching carriers. The mismatch at the interface between two dissimilar materials provides additional defects and stacking faults. The carrier lifetime due to surface recombination is usually low for untreated surface. Therefore the effective lifetime of the minority carriers is brought down in the following relationship [13].

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} \quad (3.5)$$

The surface recombination, mainly due to dangling bonds, can be regarded as traps inside the bandgap. Thus, it is also modeled by Shockley-Read-Hall recombination. The surface recombination velocity S_r , a very important parameter to characterize the surface quality, is represented by [13]

$$s_r = \frac{s_n s_p (n_{0s} + p_{0s} + \Delta n_s)}{s_n (n_{0s} + n_{1s} + \Delta n_s) + s_p (p_{0s} + p_{1s} + \Delta p_s)} \quad (3.6)$$

where n_{0s} , n_{1s} , Δn_s , are the equilibrium carrier concentration, carrier concentration at trap energy level and excess carrier concentration of electrons at the surface. The same definition applies to holes as well. s is defined as surface velocity where $s_n = \sigma_{ns} v_{th} N_{it}$ and $s_p = \sigma_{ps} v_{th} N_{it}$. σ is the capture cross section, v_{th} is the thermal velocity of the carrier and N_{it} is the interface traps density.

3.2 *u-PCD characterization*

μ -PCD is particularly popular because this method has the capability to monitor the carrier recombination dynamics without contacting the unit under test. It can easily and successfully monitor the carrier lifetimes during the processing step before the material is made into device [16]. It is even possible to measure the bulk lifetime by immersing the samples in hydrofluoric acid. This contactless measurement utilizes microwave at radio frequency to monitor the conductivity change in the sample. A short laser pulse is applied to the sample causing the generation of photo-carriers. The change in conductivity is proportional to the excess carrier concentration inside the material thus giving a rise in conductivity. A microwave signal is sent out to the sample and a detector is used to monitor the reflected microwave, which its power is proportional to the change in conductivity in the sample. Conductivity decreases as the photogenerated carriers recombine over time. By observing the conductivity decay, the lifetime of the minority carriers can be deduced.

Figure 3.1 shows an example of the measured photoconductivity decay. The conductivity can be modeled as an exponential decay function with time constant representing the carrier lifetime.

$$\sigma(t) \propto \exp\left(-\frac{1}{\tau_{eff}} t\right) \quad (3.7)$$

The carrier lifetime is modeled by two components, surface lifetime and bulk lifetime. The effective, or the measured lifetime, is governed by both surface and bulk lifetime in the following relationship.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} \quad (3.8)$$

τ_{eff} , τ_b , τ_s represents effective lifetime, bulk lifetime and surface lifetime respectively. In most cases, surface lifetime is much smaller than the bulk lifetime thus the effective lifetime is dominated by surface lifetime which is determined by the diffusion length of carriers and surface recombination velocity. The surface lifetime is typically low for bare silicon surface because there are lots of defects and dangling bonds acting as carrier traps. For an unpassivated surface of crystalline silicon, the surface recombination velocity can vary from 10^3 cm/s with well chemically polished surface to 10^5 cm/s with damaged surface from saw damage and ion implantation [17]. With well passivated surface, the surface recombination velocity can be kept below 10 cm/s. Surface passivation is thus required to suppress the trapping at the surface.

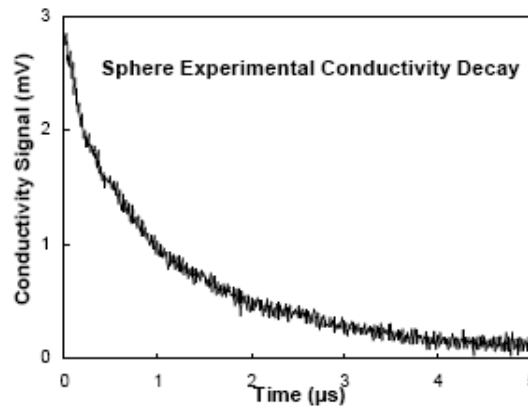


Figure 3.1. An example of a photoconductivity decay signal [18]

3.3 Theoretical Analysis of Conductivity Decay in Sphere

The μ -PCD measurement was originally designed for the planar wafer. In a planar wafer, the beam size of the laser pulse is much larger than the wafer thickness, thus the charge distribution can

be analytically calculated by one dimension model [19]. In one dimension, the continuity equation can be written as

$$\frac{\partial n(z,t)}{\partial t} = D \frac{\partial^2 \Delta n(z,t)}{\partial z^2} + G - \frac{\Delta n(z,t)}{\tau_b} \quad (3.9)$$

where D is the diffusion coefficient, G is the generation rate, τ_b is the bulk lifetime, and n is the concentration of minority carrier. z represents the spatial variation in the direction of the wafer thickness and t is the time after the laser pulse is turned off. Assuming no carrier generation in the bulk for $t > 0$, the generation rate G equals to 0. The initial and boundary conditions are [19]

$$\Delta n(z,0) = g_0 \exp(-\alpha z) \quad (3.10)$$

$$D \frac{\partial}{\partial z} \Delta n(0,t) = S_0 \Delta n(0,t) \quad (3.11)$$

$$D \frac{\partial}{\partial z} \Delta n(w,t) = -S_w \Delta n(w,t) \quad (3.12)$$

where g_0 is the initial carrier distribution at $t = 0$, S_0 and S_w are the surface recombination velocity at the front and back side of the wafer respectively, and w is the thickness of the wafer.

By solving the partial differential equation by separation of variables, the excess carrier concentration has the following profile [19].

$$\Delta n(z,t) = \sum_{i=1} \Gamma_i \left(a_i \cos(a_i z) + \frac{S_0}{D} \sin(a_i z) \right) \exp \left[- \left(\frac{1}{\tau_b} + a_i^2 D \right) t \right] \quad (3.13)$$

where a_i are the decay coefficients derived from the boundary condition and Γ_i are found by using the initial condition.

To find the average conductivity $\sigma(t)$ which the μ -PCD measures, the excess carrier density is integrated over the thickness of the wafer divided by the thickness itself [19].

$$\sigma(t) = \frac{q\mu}{w} \int_{z=0}^w \Delta n(z,t) dz \quad (3.14)$$

By similar approach, the charge kinetic inside the sphere can be deduced. However, there are several complexities in spherical geometry. First, the continuity equation is now written in spherical coordinate [18].

$$\frac{\partial \Delta n}{\partial t} = D \left[\frac{1}{r^2} \frac{\partial}{\partial r} \left(r^2 \frac{\partial \Delta n}{\partial r} \right) + \frac{1}{r^2 \sin \theta} \frac{\partial}{\partial \theta} \left(\sin \theta \frac{\partial \Delta n}{\partial \theta} \right) \right] - \frac{\Delta n}{\tau_b} \quad (3.15)$$

where r is the radius, θ is the zenith angle. The azimuth angle ϕ dependency is eliminated because of the symmetry. Instead of having one dimensional continuity equation, two dimensional continuity equation arises from non-planar geometry. The boundary conditions rule out the spherical Bessel and Legendre function of the second kind in the final solution. The boundary condition regarding the surface recombination velocity is

$$\frac{D\lambda}{SR} + \frac{j_m(\lambda)}{j'_m(\lambda)} = 0, \quad m = 0, 1, 2, \dots \quad (3.16)$$

where D is the diffusion coefficient, R is the radius of the sphere, S is the surface recombination velocity, $j_m(\lambda)$ and $j'_m(\lambda)$ are the spherical Bessel function and its derivative. λ/R , the coefficient coming from the separation of variables of the partial differential equation, is a coefficient normalized by the radius which is similar to a_i in the planar case. This expression is solved numerically to find the value of λ . There exists infinite number of roots in (3.16) thus for each order m , there are infinite number of modes i for λ . The final form of excess carrier distribution is

$$\Delta n(r, \theta) = \sum_m \sum_i \Gamma_{m,i} \exp \left[- \left(\frac{1}{\tau_b} + D \frac{\lambda_{m,i}^2}{R^2} \right) t \right] j_m \left(\lambda_{m,i} \frac{r}{R} \right) P_m(\cos \theta) \quad (3.17)$$

where $j_m(x)$ is the spherical Bessel function and $P_m(x)$ is the Legendre function of the first kind and m is the order with value of 0, 1, 2, ... and i is the mode with value of 1, 2, 3, ... To calculate the

conductivity, the integration is carried out over the entire volume of sphere.

$$\sigma(t) = \frac{q\mu}{V} \int_0^{2\pi} \int_0^{\pi} \int_0^R \Delta n(r, \theta) r^2 \sin \theta dr d\theta d\phi \quad (3.18)$$

where q is the electron charge, μ is the mobility of the carriers. Another complication coming from the non-planar geometry is the initial charge distribution. The angle at which the light ray enters the sphere changes along the sphere surface. With the light being refracted, the ray becomes concentrated at a focal point near the center. These two effects are depicted in Figure 3.2.

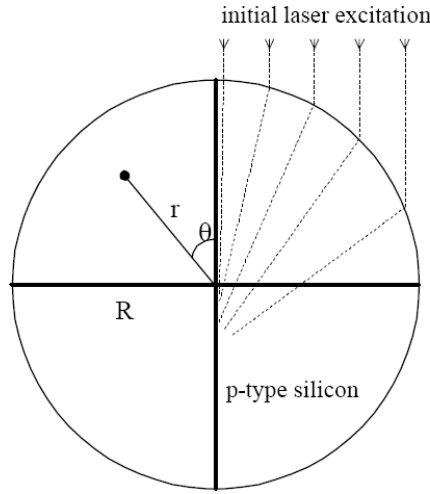


Figure 3.2. A sphere under laser excitation depicting how rays enter the sphere [18]

The new expression of the initial carrier concentration takes into the account of the focusing effect ($1/r^2$) and reduced intensity at a tilted angle ($\cos\theta$).

$$\Delta n(r, \theta, 0) = g_0 \frac{1}{r^2} \cos \theta \exp(-\alpha(R - r)) \quad (3.19)$$

The above expression is only an approximation but not a realistic model because the carrier concentration is finite inside the sphere. This expression (3.19) blows up when $r = 0$. Also, the focal point is not exactly located at the center. (3.19) is valid for the upper hemisphere only. At the lower hemisphere, no light should enter through the sphere surface. However, the carriers

from the upper hemisphere can be injected into the lower hemisphere. Thus the expression for the lower hemisphere become

$$\Delta n(r, \theta, 0) = g_0 \frac{1}{r^2} \cos(\pi - \theta) \exp(-\alpha(R + r)) \quad (3.20)$$

In the planar wafer, the coefficient Γ_i can be found analytically and the expression is listed in [19].

To find Γ for sphere, the treatment is much more complicated because the integration of the spherical Bessel function cannot be analytically determined. The average conductivity of a sphere is

$$\sigma(t) = \frac{q\mu}{V} \sum_m \sum_i \Psi_{m,i} \exp \left[- \left(D \left(\frac{\lambda_{m,i}}{R} \right)^2 + \frac{1}{\tau_b} \right) t \right] \quad (3.21)$$

$$\begin{aligned} \text{where } \Psi_{m,i} = & \Gamma_{m,i,u} \int_0^R j_m(\lambda_{m,i} \frac{r}{R}) r^2 dr \int_0^{\pi/2} P_m(\cos \theta) \sin \theta d\theta \int_0^{2\pi} d\phi \\ & + \Gamma_{m,i,l} \int_0^R j_m(\lambda_{m,i} \frac{r}{R}) r^2 dr \int_{\pi/2}^{\pi} P_m(\cos \theta) \sin \theta d\theta \int_0^{2\pi} d\phi \end{aligned} \quad (3.22)$$

$\Psi_{m,i}$ represents the decay coefficients of different orders and modes in the average conductivity. A few simplifications can be made based on $\Psi_{m,i}$ to reduce the amount of integration. The details are outlined in Appendix A. Table 3.1 shows a few values of Γ . The Γ is calculated using surface recombination velocity of 10000 cm/s, radius 0.04 cm, and absorption depth of 0.0032 cm. The value of Γ is normalized by the zeroth order fundamental mode. The overall Γ , however, has a larger value for the first order fundamental mode compared to zeroth order fundamental mode. Although Γ shows significant contribution from higher orders and modes in the excess carrier distribution, the zeroth order fundamental mode may still be the dominant exponential in the average conductivity.

Table 3.1. Value of Γ for the first few modes

Order, mode	λ	Γ	Γ normalized
0, 1	2.910	4.808	1.00
0, 2	5.841	8.303	1.73
0, 3	8.805	18.16	3.78
1, 1	4.166	9.25	1.92
1, 2	7.195	12.27	2.55

Finally $\Psi_{m,i}$ can be determined by integrating the spherical Bessel function over the radius and Legendre function over θ in Equation (3.22). Only the orders $m = 0$ and 1 remain after the integration. The value of $\Psi_{m,i}$ are listed in Table 3.2.

Table 3.2. Value of the decay coefficient $\Psi_{m,i}$

m,i	Γ	Ψ	Ψ normalized
0, 1	4.808	2.40×10^{-4}	1.0
0, 2	8.303	-9.60×10^{-5}	-0.40
0, 3	18.16	8.34×10^{-5}	0.35
1, 1	9.25	1.70×10^{-4}	0.71
1, 2	12.27	3.28×10^{-5}	-0.14

3.3.1 Interpretation of Conductivity Decay Coefficients

As seen in Table 3.2, the decay coefficient of conductivity in the charge kinetic is still dominated by zeroth order fundamental mode. However, the higher orders and modes do not decay quickly.

The next dominant mode is the first order fundamental mode.

By graphing the conductivity decay using the normalized coefficients in Table 3.2 and a bulk lifetime of $5 \mu\text{s}$, it can be seen in Figure 3.3 that higher order fundamental mode gives a faster decay than just the zeroth order fundamental mode. In fact, using only fundamental modes from order 0

and 1 approaches the approximation of using more terms in higher modes. Thus the overall conductivity decay can be very well described by the fundamental modes of order 0 and 1.

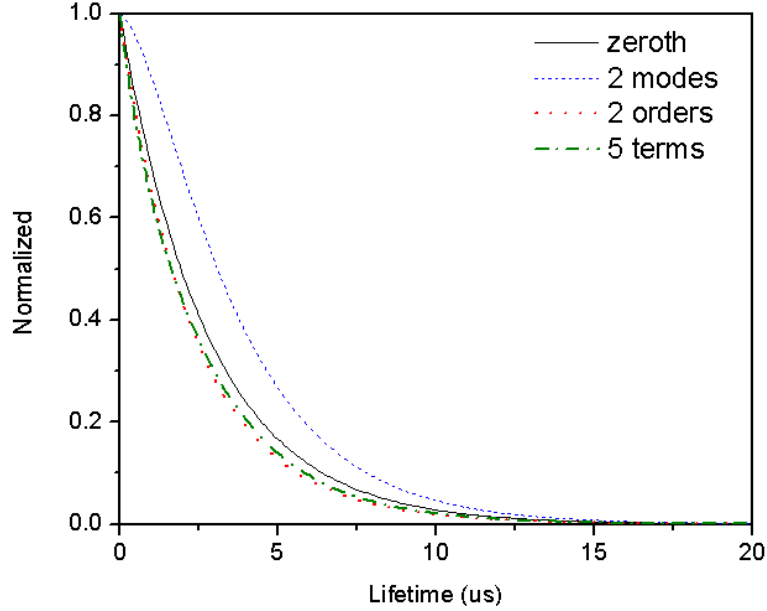
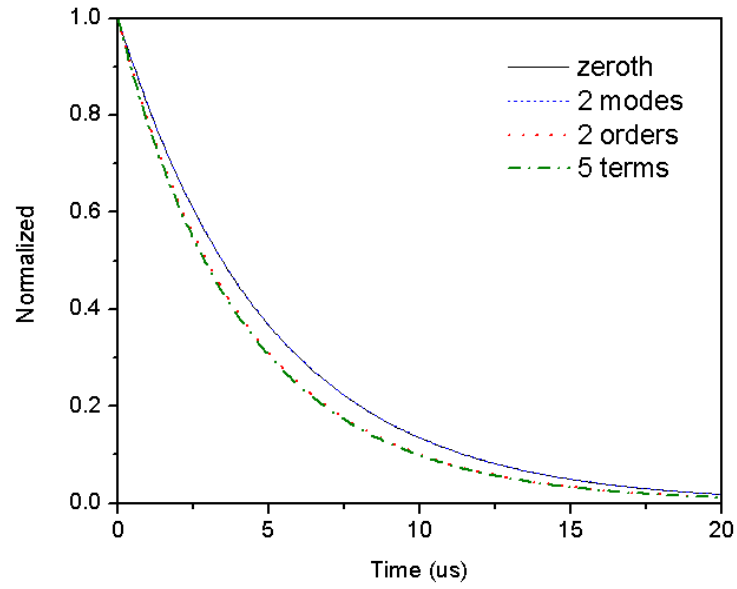


Figure 3.3. Calculated photoconductivity decay response with different approximations (a) only zeroth order fundamental mode (b) first two modes from zeroth order (c) fundamental modes from zeroth and first order (d) total of five modes from zeroth and first order

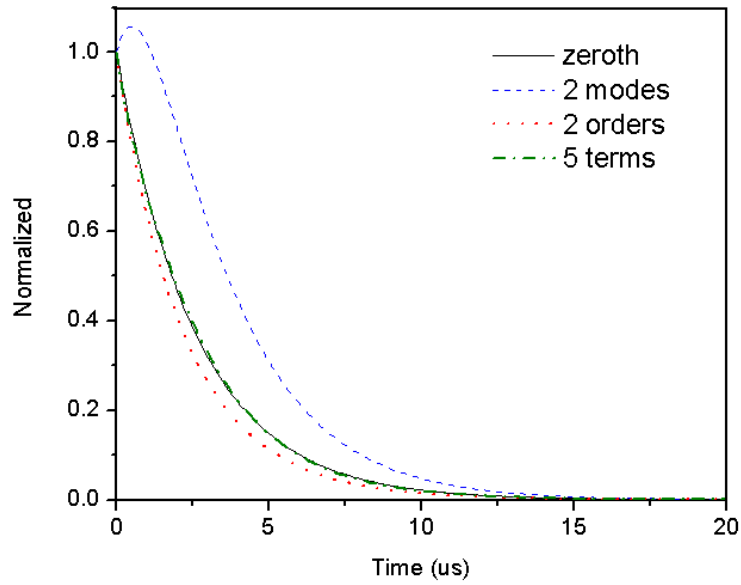
3.3.2 Effect of Surface Recombination Velocity on Photoconductivity Decay

The surface recombination velocity is a key component in determining the decay constant λ [18]. A list of λ and Ψ , the decay coefficients for different surface recombination velocities, are found in Appendix B. For very low surface recombination velocity ($S = 10$ or 100 cm/s), the zeroth order first mode has a very small decay constant, while all the other constants are a few times larger. It means the effect of higher modes fade out quickly. Looking at the decay coefficients, only Ψ of zeroth order fundamental mode and first order fundamental mode contribute to the overall conductivity. The higher modes have extremely small decay coefficients which do not affect the overall photoconductivity as shown in Figure 3.4 (a). For high surface recombination velocity ($S = 10^5$ to 10^6 cm/s), the decay constant of the zeroth order first mode is large and it is comparable to decay constants of higher orders and modes. The calculation of Ψ also shows that in addition to

the fundamental modes of zeroth and first order, higher modes have decay coefficients large enough to be comparable to the decay coefficients of fundamental modes. As a result, the overall conductivity cannot be reduced to only two fundamental exponentials. With 5 modes approximation, the curve is different from the response obtained from solely zeroth and first order fundamental modes as shown in Figure 3.4 (b).



(a)



(b)

Figure 3.4. Calculated photoconductivity with different approximations for (a) low surface recombination velocity ($S = 10$ cm/s) (b) high surface recombination velocity ($S = 10^5$ cm/s)

3.4 Lifetime Measurement in Spherical Silicon

Although μ -PCD technique was originally developed for planar technology, it has been very well adopted in spherical silicon. Some papers have reported ways to measure response from individual spheres as well as a collection of spheres [20, 21]. The measurement set up is shown in Figure 3.5. It measures the response from a number of spheres so the measurement results will be the average values coming from a large number of samples.

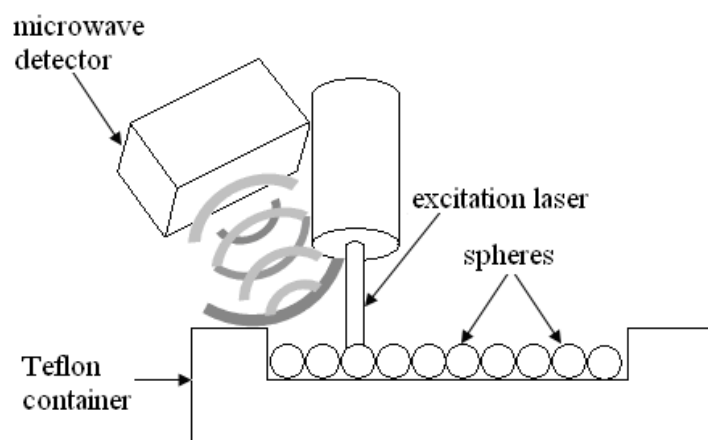


Figure 3.5. Set up of the μ -PCD measurement for spherical silicon

3.5 Rapid Thermal Oxide Passivation of Spherical Silicon

Silicon dioxide grown by Rapid Thermal Oxidation (RTO) has been used as a passivation material for planar solar cell to increase cell efficiency [22, 23]. To investigate the effect of rapid thermally grown silicon dioxide passivation in spherical silicon, a set of high quality spheres with lifetime of $1.5\ \mu\text{s}$ without passivation and lifetime of $1.8\ \mu\text{s}$ with hydrofluoric acid passivation will be used to study the surface recombination effect. Another set of low quality spheres which has a lifetime of $0.13\ \mu\text{s}$ without passivation is also included to observe the high temperature effect. The bulk quality of $0.28\ \mu\text{s}$ was concluded by measuring the spheres in hydrofluoric acid.

In the first attempt, the spheres were subjected to a high temperature treatment of $900\ ^\circ\text{C}$ in oxygen ambient in rapid thermal processing (RTP) system for 5 minutes. In RTP, the ramping of

temperature can go up or cool down at a rate as fast as 100 °C / second. Although an oxide is grown on the surface serving as passivation layer, the measured effective lifetime has degraded to 0.7 μ s. The degradation in lifetime after high temperature oxidation step can have two implications. The bulk quality has changed or the passivation effect has altered or both. In an attempt to improve the quality of the grown oxide, another stack of spheres is oxidized at 900 °C in rapid thermal system for 5 minutes with controlled cooling where the spheres are cooled down by step of 50 °C and hold for 20 seconds. This time the measurement shows an improved lifetime of 0.86 μ s attributed to better oxide quality from controlled cooling. The slow cooling can improve oxide quality by inducing a smoother Si-SiO₂ interface [24]. In addition, the nitrogen anneal helps to reduce the interface state density. To further optimize the oxide quality, a new stack of spheres are oxidized at the same temperature for 2.5 minutes followed by nitrogen anneal at 950 °C for another 2.5 minutes with controlled cooling. The temperature profile is shown in Figure 3.6. The measured lifetime is 1.0 μ s, which shows noticeable improvement over the previous oxidized stacks. To investigate the effectiveness of the annealing, the oxide layer of the annealed stack is removed by immersing the spheres in hydrofluoric acid. With bare surface after oxide is stripped, the μ -PCD signal gives a reading of 0.90 μ s. The stripped oxide spheres which were immersed in hydrofluoric acid achieve a measured lifetime of 1.0 μ s implying the spheres possess a bulk lifetime of 1.0 μ s. Since the bulk lifetime is essentially the same as the lifetime measured from oxidized spheres with nitrogen annealing, it can be concluded that oxidation with nitrogen anneal and controlled cooling can suppress surface recombination and thus the bulk lifetime dominates. However, this experiment also shows that the bulk quality has degraded through thermal oxidation. The result is summarized in Figure 3.7.

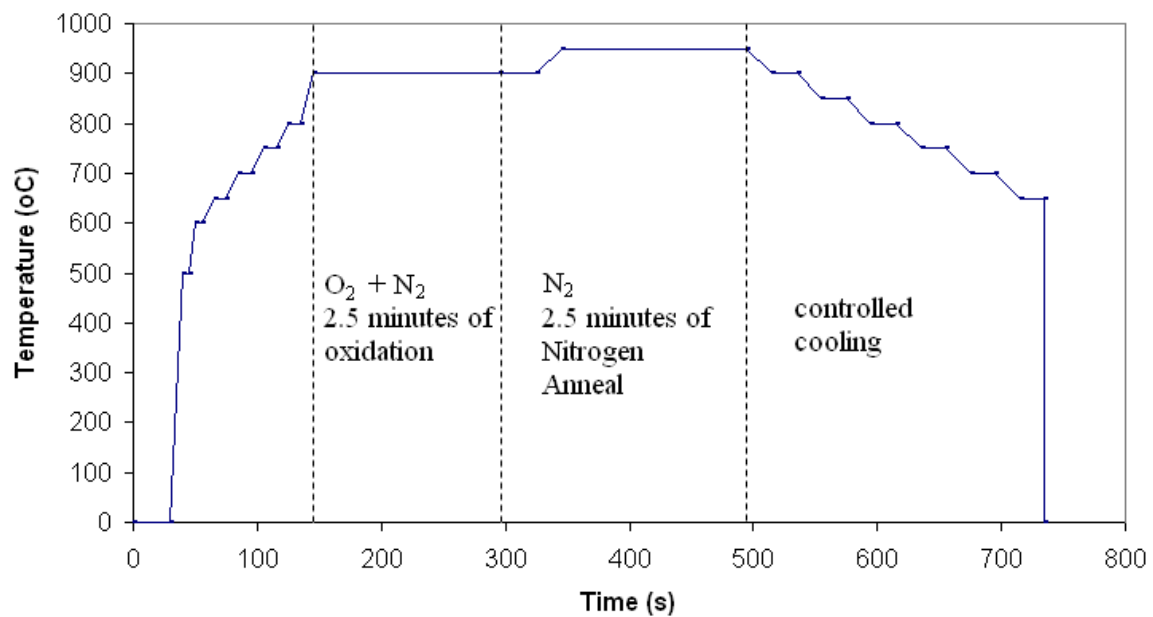


Figure 3.6. Temperature profile of thermal oxidation with nitrogen anneal and controlled cooling

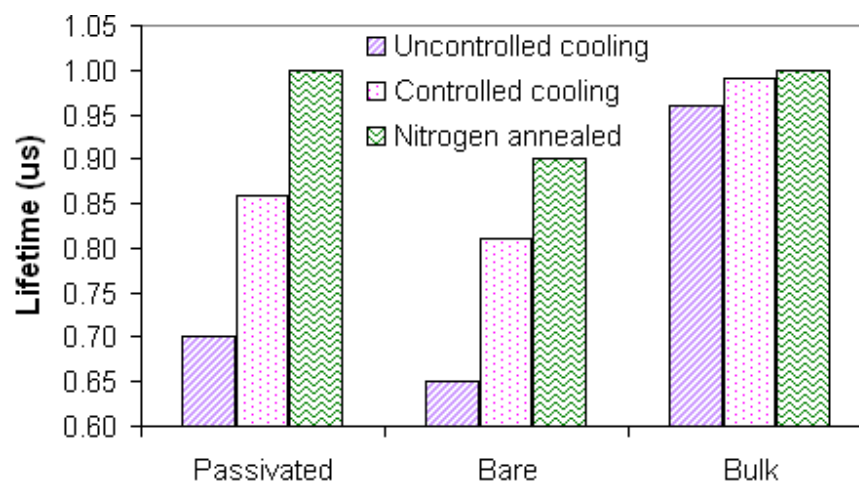


Figure 3.7. Lifetime of different quality of oxide passivation at 900°C. (stripe) 5 minutes oxide with rapid cooling, (dot) 5 minutes oxide with controlled step cooling, (wave) 2.5 minutes oxide with 2.5 minutes nitrogen anneal at 950°C with controlling step cooling

The same set of experiment described above is carried out on the low quality spheres. The results in Figure 3.8 show similar trend as the result with high quality spheres. By exposing the spheres at high temperature oxidation with nitrogen anneal, the lifetime measurement gives $0.37 \mu\text{s}$ which implies this oxide passivation works well on low quality spheres. The high temperature treatment has a positive effect on low quality spheres. It is suggested by the evidence of a better bulk lifetime after high temperature annealing.

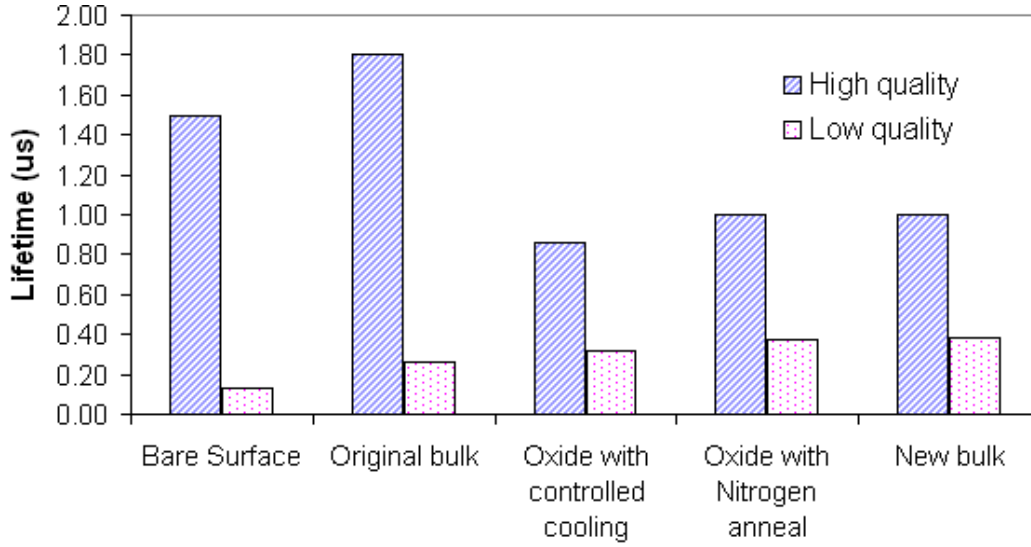


Figure 3.8. Lifetime of different quality of oxide passivation. (stripe) high quality sphere, (dot) low quality sphere

From the result of the two experiments, thermal oxidation with nitrogen anneal and controlled cooling can suppress surface recombination effectively. The issue with this method is that the bulk quality is altered at the same time due to high temperature treatment. Depending on the original bulk quality, the bulk can improve or degrade after the treatment of rapid thermal oxidation. The bulk lifetime of better quality spheres before annealing was 1.8 μs but it has degraded to 1.0 μs after annealing. It is proven that high temperature oxidation can cause thermal degradation in solar grade multicrystalline silicon [25]. The degradation occurs at the region where the dislocation density is high and the high temperature tends to drive impurities to the dislocation. The bulk degradation from high temperature treatment only happens in multicrystalline silicon (mc-Si), implying the sphere may have similar properties as mc-Si [26]. On the other hand, the high temperature treatment improves the bulk quality of the low quality spheres as some of the impurities may have been gettered [27]. In the case where the bulk quality is degraded, it is believed that the solar cell can still operate at a higher open circuit voltage relative to the one with bare surface. This assumption is made based on the fact that the p-n junction is a shallow junction. The surface passivation can reduce surface recombination such that more carriers which diffuse to the surface can reach the contact without recombination, resulting in a higher open circuit voltage.

3.6 Summary

The theoretical analysis of excess carrier distribution shows that first order fundamental mode has a significant contribution to the photoconductivity decay in addition to the zeroth order fundamental mode. Therefore, the curve fit of one exponential curve is not sufficient to approximate the photoconductivity decay in silicon sphere.

With the use of μ -PCD, the surface passivation effect of rapid thermal oxide is examined. The combination of high temperature (900 °C) oxide growth with nitrogen anneal and controlled cooling forms a high quality oxide at the surface to passivate surface states. The high temperature step, on the other hand, has an unknown effect on the quality of the spheres. In the case where high quality spheres are passivated, the bulk quality degrades after high temperature treatment. For low quality spheres, the bulk carrier lifetime indeed improves after oxidation. Nonetheless, suppressing surface recombination is imperative for shallow emitter to possess high open circuit voltage. In addition to thermal oxide, low temperature deposited silicon nitride is also an excellent choice for sphere passivation and should further be investigated.

Chapter 4

Novel Spherical Device Technology

In current spherical photovoltaic technology, a p-n junction is formed near the sphere surface by vapour diffusion of phosphorous trichloride oxide (POCl_3) on a p-type sphere [28]. The emitter diffusion however is a high temperature step carried out at 925 °C for 40 minutes. The resultant junction depth is about 0.5 μm which is considered very thick. A thick emitter may absorb a considerable amount of high energy photons as their absorption depth is below 1 μm . The emitter layer heavily doped with about $10^{19}/\text{cm}^3$ results in short carrier diffusion length and promotes Shockley-Read-Hall and Auger recombination [29]. Consequently, the thick emitter requires selective etching to thin down the emitter at the top of the sphere for better performance. The high temperature and extra etching steps incur additional cost to the fabrication process of the promising low-cost spherical solar cell. Instead of high temperature diffusion, Plasma Enhanced Chemical Vapour Deposition (PECVD) is used to form a thin emitter layer on sphere surface. This low temperature step of about 300 °C can reduce the thermal budget, as well as provide excellent control in emitter layer thickness.

4.1 Device Design and Process Flow

The unconventional geometry of sphere results in a new device structure. The difference between spherical diode and planar diode is depicted in Figure 4.1. In fabrication of new device structure, a new design of fabrication process is required because some of the steps in planar device fabrication cannot be directly converted to equivalent spherical process. For example, PECVD deposition parameters need to be optimized for covering non-planar surface. Deposition of contact layer is non-trivial for minuscule silicon balls. Some complications may exist in lithography process such as spin coating photoresist and mask alignment. With these difficulties in current fabrication

process, a new simple fabrication process flow specialized for spherical device must be developed.

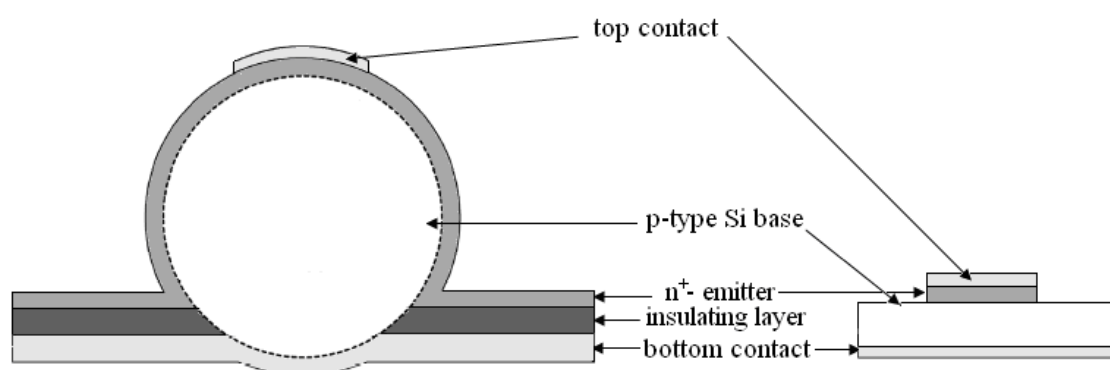


Figure 4.1. A schematic showing different structures for spherical and planar diode

A proposed process flow for spherical device is outlined in Figure 4.2 in parallel with the process flow for planar device. To solve the problem of depositing back contact on individual sphere, an aluminum foil is used to provide mechanical support for an array of spheres. A Rapid Thermal Process (RTP) at about 620 °C for 60 – 90 seconds can bond the spheres onto the aluminum substrate. The eutectic temperature and the duration of bonding vary depending on the impurity level of the substrate and the pressure applied onto the spheres. To clean silicon wafer, a RCA 1 cleaning should be performed prior to any deposition on silicon surface. The purpose of RCA 1 is to remove any organic substances on the surface. This process involves heating the wafers in a solution containing hydrogen peroxide, ammonia and deionized water in the ratio of 1: 1: 4 for 13 minutes. However, this process cannot be carried out because the spheres are already bonded onto the aluminum substrate. The implementation of RCA 1 may lead to contamination by the impurities in aluminum. Instead a simple acetone followed by propanol rinse serves the purpose of removing organic substances. A hydrofluoric acid (HF) dip is carried out to remove any oxide layer before deposition.

In order to isolate the back contact from the emitter layer, an insulating layer is required to prevent the emitter layer touching the back contact directly. There is a wide selection of insulating

materials and the development of insulation for spherical device will be discussed thoroughly in section 4.5. After insulator deposition, the top hemisphere of the sphere must be exposed for emitter formation. Depending on the insulation technology used, different approaches are applied to expose the surface. This will again be discussed in section 4.5.

The substrate is then loaded into PECVD chamber for emitter layer deposition. A 5-minute hydrogen (H_2) plasma treatment is performed in the same process before n^+ layer deposition. The H_2 plasma treatment can clean the surface of the sphere, especially in the case where RCA cleaning process is not applicable. It has been proven that H_2 plasma treatment can reduce the recombination at the interface [30]. The deposition parameters for low temperature film deposition have been optimized for planar wafer. For planar surface, the roughness of the surface is not a concern. However, the surface for deposition is not smooth and flat in spherical technology. Due to non-planar geometry, the deposition parameters should be adjusted to accommodate the new structure. The detail of emitter layer development is found in section 4.4.

In planar technology, lithography would be used to define contact area. However, designing a mask for spherical device may require lots of efforts and justification. For contact deposition a shallow mask is employed instead. The shallow mask has holes right above the top of the spheres which allow the sputtered atoms to be deposited on the spheres under the mask. The whole device process is completed after the sputtering step. In planar diode, a few extra steps will follow up after deposition of top metal contact. The diode areas are patterned by lithography step where extra aluminum is etched away. For the purpose of testing, the exposed emitter layers not covered by metal contact are etched away by Reactive Ion Etching (RIE) to create individual mesa diode. Finally, a metal layer is deposited at the back of the wafer to make a back contact. Except for a few essential steps, the process flow for spherical diode is different from that for planar diode. The process parameters should be optimized for spherical geometry.

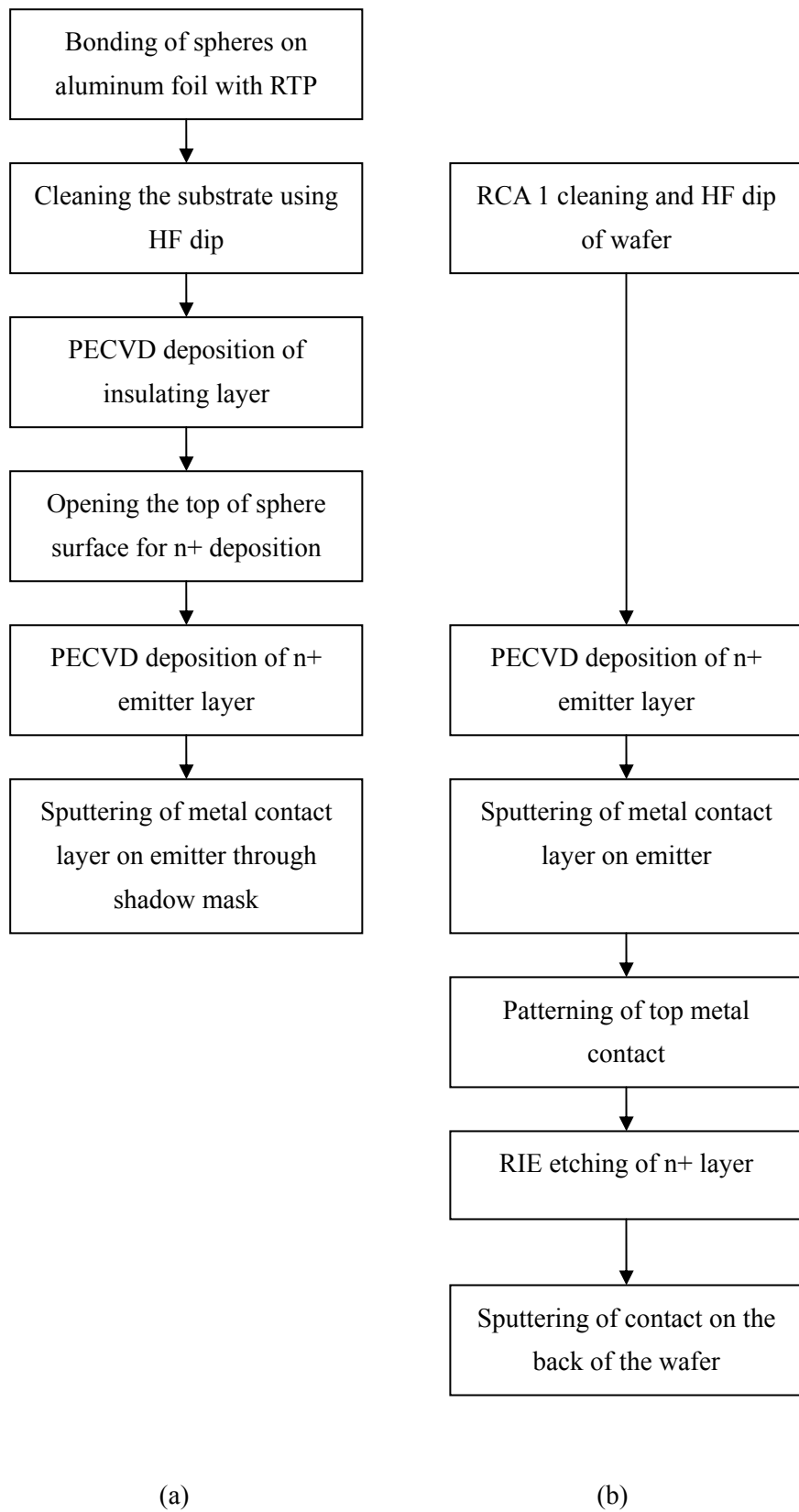


Figure 4.2. The process flow of (a) spherical device (b) planar device

4.2 Experimental Setup

A simple test structure, shown in Figure 4.3, was developed for research purpose. P-type silicon spheres of about 1 mm in diameter are bonded to a thin aluminum disk of 0.4 mm thickness which acts as mechanical support and back contact. The bonding is carried out in Rapid Thermal Processing (RTP) chamber with temperature of 620 °C for 90 seconds. At the interface between the sphere and aluminum disk, silicide which can be modeled at p+ silicon is formed at the eutectic temperature. The sample can then be loaded in the chamber for emitter deposition. An aluminum contact layer is sputtered on top of the sphere using a shadow mask to eliminate the complication of performing photolithography on non-planar surface. It is important to note that the p-type spheres used for the subsequent experiment is of low quality because μ -PCD measurement cannot give a lifetime due to low conductivity signal. Better quality spheres were not available at the time of experiment.

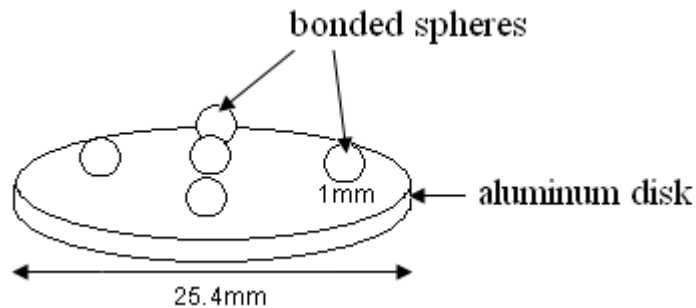


Figure 4.3. Silicon spheres bonded on aluminum substrate

4.3 Low Temperature Epitaxial Film as Emitter layer for Planar Technology

In previous literatures, depositing n+ emitter using Plasma Enhanced Chemical Vapour Deposition (PECVD) on silicon wafer has been demonstrated. PECVD, which is a low temperature technique, has first been used to deposit amorphous materials such as amorphous silicon and silicon nitride [9, 31]. In the recent development of silicon thin film, PECVD process has been evolved to be able to

deposit microcrystalline and nanocrystalline silicon film by controlling hydrogen dilution [10 – 12]. Recently it has been reported that a quasi-epitaxial film with close to single crystallinity has been deposited on multicrystalline silicon substrate for photovoltaic applications [32]. With similar approach, experiments are performed to attempt the deposition of quasi-epitaxial layer on silicon sphere.

Two emitter thin films developed previously for planar silicon wafer were proven to have good electrical properties. The first film has a 92 % hydrogen dilution and the other one has a 99% dilution. The deposition conditions are found in Table 4.1. Both of the films will be investigated on silicon sphere.

Table 4.1. PECVD parameters for low temperature film deposition

Hydrogen dilution	H ₂	SiH ₄	PH ₃	Pressure	Power	Temperature
92 %	275 sccm	25 sccm	10 sccm	400 mTorr	60 mW/cm ²	300 °C
99 %	500 sccm	5 sccm	5 sccm	900 mTorr	70 mW/cm ²	300 °C

4.4 Development of Low Temperature Epitaxial Film for Spherical Technology without Insulation

PECVD was designed to perform thin film deposition on planar surface. As its use becomes ubiquitous in thin film technology, this technique has been adopted to deposit different materials on advance structure with certain features. As sphere is not a planar surface, the uniformity of the deposited film is a concern. On the other hand, the non-uniform coverage of the deposited film may be advantageous for the novel device. Although low temperature epitaxial film shows excellent crystallinity on planar device, this hypothesis should be verified for spherical silicon. Some complications from spherical device are the quality of the silicon sphere and crystal orientation of the surface which may have undesirable effect on the quasi-epitaxial growth.

4.4.1 Directionality

In the initial design where an appropriate insulating technique has not been developed, there exists a challenge in isolating the highly conductive emitter layer from the substrate as shown in Figure 4.4 (a). Since the emitter film is in contact with the aluminum substrate, the current would travel a less resistive path from n⁺ layer directly to the substrate, bypassing the sphere. One of the features arises from spherical geometry is that thin film deposition is not uniform across the whole sphere surface. As a result, the lower hemisphere may not even have thin film deposited due to self-masking effect. The non-conformal deposition is advantageous in isolating the emitter layer and the substrate in spherical diode. The self-masking effect can be guaranteed provided that the deposition is directional as demonstrated in Figure 4.4 (b). It is assumed that in directional deposition the incoming radicals should arrive vertically to the sphere surface. Under this condition, the self-masking effect should block the radicals from approaching the surface of the lower hemisphere.

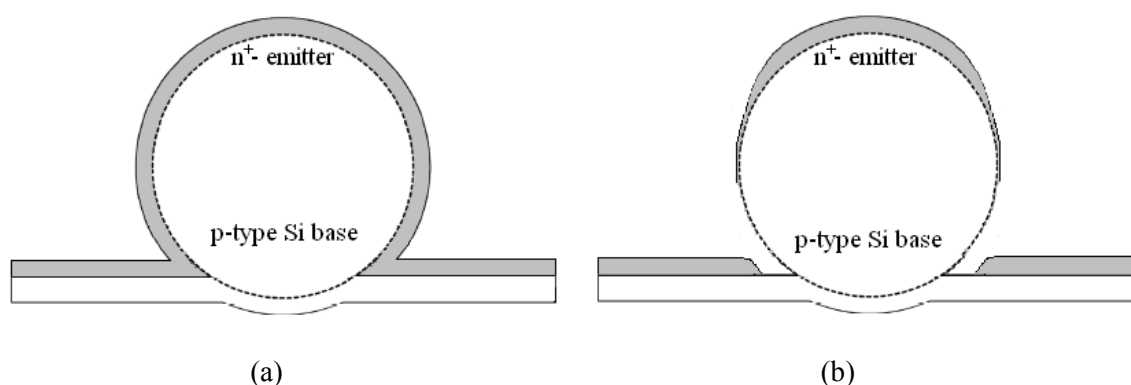


Figure 4.4. Schematic of test structure after n⁺ deposition (a) conformal deposition (b) directional deposition

4.4.2 Optimal Thickness

As mentioned in the beginning of this section, n⁺ emitter diffusion gives a thick emitter therefore etching step is required to be performed to thin down the emitter layer. With PECVD deposition, the thickness of the n⁺ layer can be very well controlled by the deposition time. However some

considerations should be accounted for. First, PECVD deposition is a low temperature process which promotes amorphous growth. Although the crystallinity can be controlled by hydrogen to silane ratio, the resulting film is not purely single crystalline. For quasi-epitaxial deposition on silicon wafer, the first few layers from the interface build on the crystalline structure at the surface and the film results in crystalline growth. As the layers are further away from the interface, the crystallinity of the film can no longer be preserved and consequently results in columnar growth. Figure 4.5 shows a high resolution transmission electron microscope (HRTEM) image of a quasi-epitaxial film grown on top of a planar multicrystalline substrate. Although the deposition parameters are different from the ones in this thesis, this figure demonstrates how the growth occurs in quasi-epitaxial deposition. To examine the film quality, a transmission electron microscope (TEM) image of the n+ film on sphere should be conducted. However, this characterization has not been carried out due to technical difficulties in preparation process associated with spherical geometry.

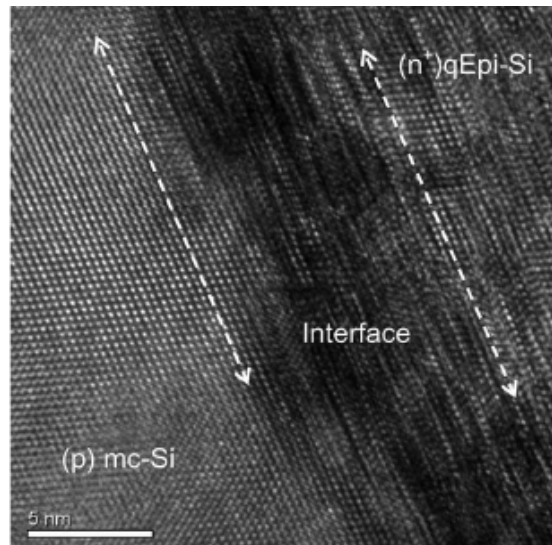


Figure 4.5. A HRTEM image of quasi-epitaxial film deposited on top of multicrystalline substrate [32]

In [32], it has proven that the quasi-epitaxial growth can extend to at least 50 nm from the interface thus this thickness is chosen for n+ emitter in this study. To replicate the experiment, an emitter

thickness of 50 nm is targeted. The deposition rate of the new recipe has not been characterized thus the exact thickness cannot be determined. One way to get the thickness of the film and as well characterize the interface is through the use of TEM. For experimental purpose, deposition time is used as a controlling variable instead.

4.5 Development of Insulating Layer for Spherical Technology

At this point, the deposition of the n^+ emitter layer relies on the self-masking effect with directional deposition to prevent a continuous n^+ film extending from the top of the sphere to the substrate. However, the emitter layer is not deposited on the side of the sphere, which drastically reduces the available junction area. An ideal structure would be similar to the one presented in Figure 4.6. Although it is assumed that no n^+ film is deposited below the lower hemisphere, this assumption may not be valid since there is a probability that the radicals get deposited on the lower hemisphere. It can be seen from the high reverse current in current-voltage characteristic presented in section 5. Therefore, an insulating layer must be developed to isolate the emitter film from the substrate. In the following subsections, two insulating schemes, spin-on-glass and silicon nitride, are introduced and investigated.

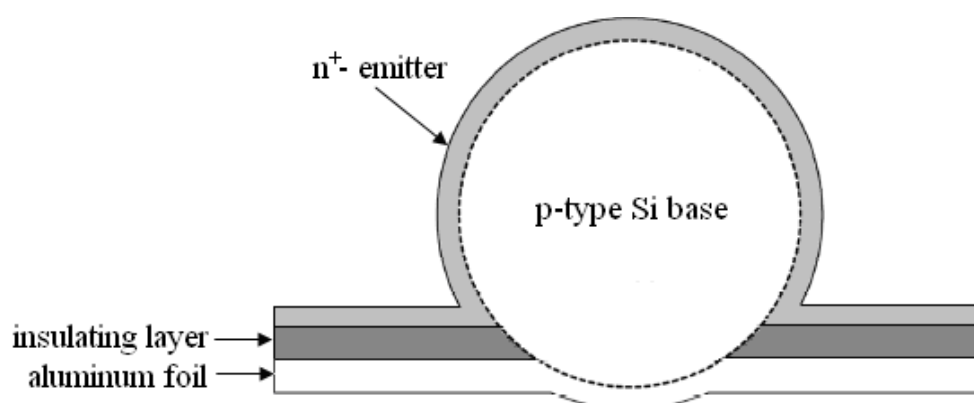


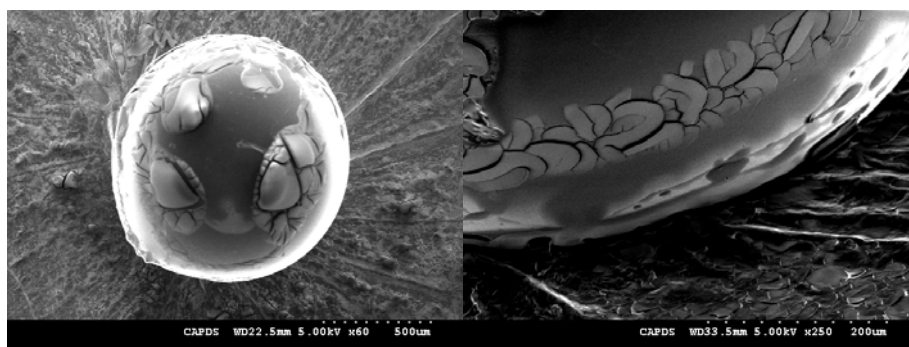
Figure 4.6. A typical design of spherical solar cell

4.5.1 Spin-On-Glass

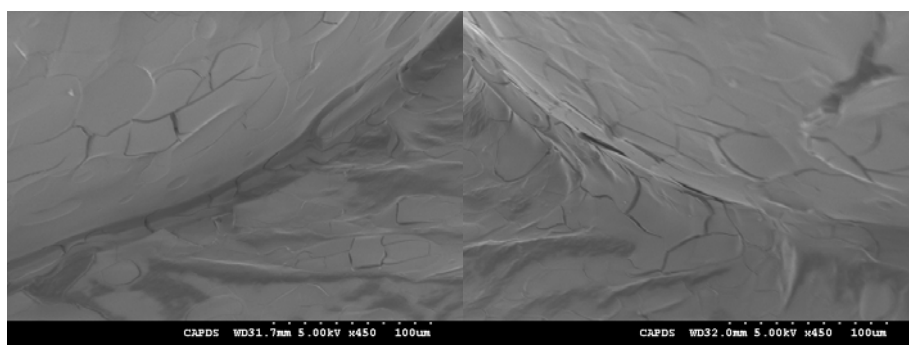
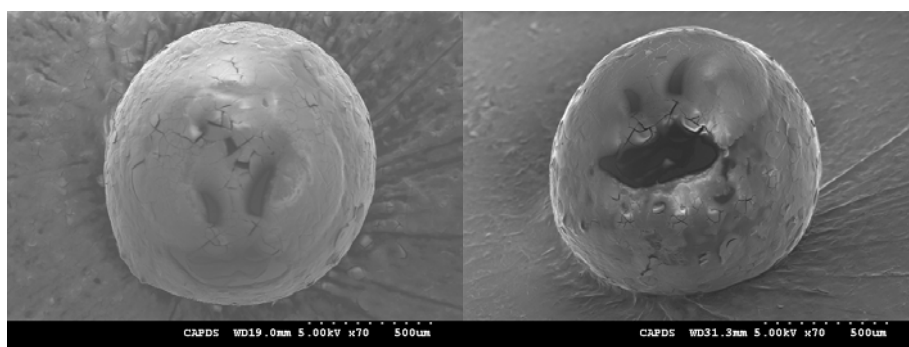
Spin-on-Glass (SOG) becomes the first candidate because of its popular use in Complementary Metal Oxide Semiconductor (CMOS) technology as a dielectric filling up trenches and planarizing intermediate layers [33]. After proper spin casting and curing, a layer of silicon dioxide is left behind.

To apply SOG as insulation, a suitable amount of SOG solvent is dropped using syringe to the aluminum substrate with spheres bonded on top. Then the substrate is spun in a spinner at a speed of 3500 rpm for 30 seconds. A thin layer of SOG remains on the substrate. To evaporate the solvent, a 2-minute 90 °C bake followed by a 2-minute 120 °C bake is used. A high temperature curing of 220 °C is performed for 1 hour then the substrate is ready for another layer of SOG application. A few layers of SOG are required since the SOG layer is only a few hundred nanometers thick after high speed spinning. Thickness of above 1 μm is desired for better isolation. Because the spheres were bonded before the application of SOG, a considerable amount of SOG sticks on the sphere surface. To clean the surface for emitter deposition, a hydrofluoric acid (HF) wipe is performed to remove any oxide including both spin-on and native oxide.

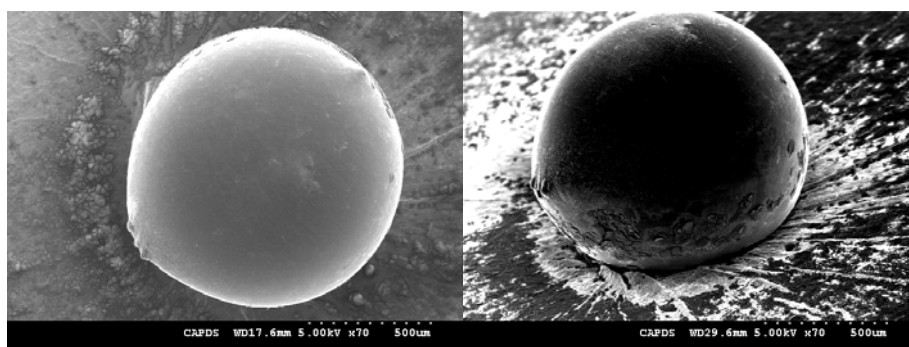
Figure 4.7 shows a number of Scanning Electron Microscope (SEM) images monitoring the process of SOG application. After one layer of SOG is spun, there is rarely any insulating layer found on the substrate. At the interface, no SOG is visible between the sphere and the substrate. After five layers of spin-coating, a visible amount of SOG covers the substrate and the sphere surface as well. At this point the interface is very well covered by insulating materials. After wiping with HF, a nice clean sphere surface is exposed. However, the SOG layers around the spheres have disappeared and the insulating layer is no longer adhered to the bonding interface.

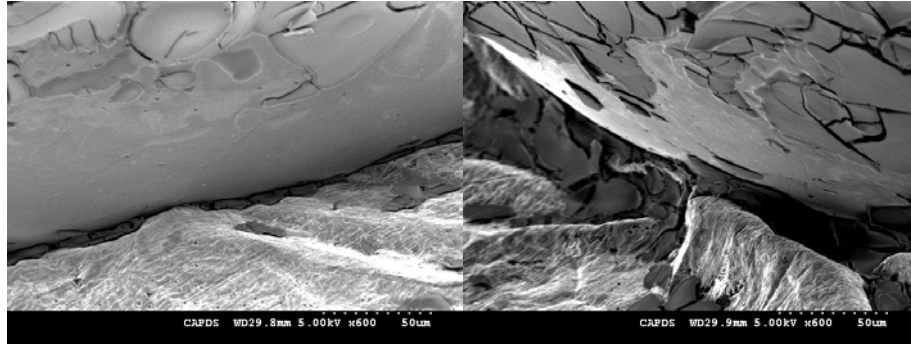


(a)



(b)





(c)

Figure 4.7. Scanning electron microscope pictures of spheres with SOG deposition (a) 1 layer (b) 5 layers (c) After HF wipe

The first concern of this technique is that spinning posts a question in conformality and uniformity. If the surface is rough, the spincoated layer will unlikely be deposited uniformly. The aluminum substrate contains lots of grinding marks from manufacturing, which are well visible without the use of microscope. This rough surface presents a great challenge for spinning material to adhere on the surface. Another reason why application of SOG on metal surface has not been successful is that SOG cannot adhere well on metal due to different thermal expansion rates [34]. As evident in Figure 4.8, the film, which is more appropriate to be described as fragments of SOG flakes, contains many cracks. The flakes may be caused by oxidation which can be suppressed by curing in nitrogen ambient [34]. This imposes a question where the layers can still perform as a good insulating layer. The real problem occurs when HF wipe is performed. HF is a very reactive acid and it can etch oxide even in its vapour form. Although the wiping was done at the top of the sphere, HF vapour can easily remove the surrounding SOG because the dimension of the sphere is very small. Interface between the sphere and the substrate is the most critical part but the insulating layer is no longer present to protect the interface after HF cleaning, as shown in Figure 4.7 (c). Due to these limitations, SOG is discarded as a successful insulating material in short term consideration.

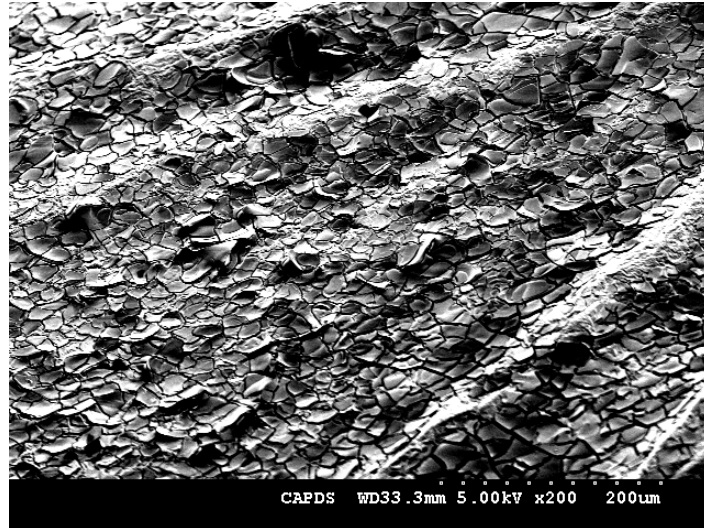


Figure 4.8. A magnified image of the SOG on the substrate

4.5.2 Silicon Nitride

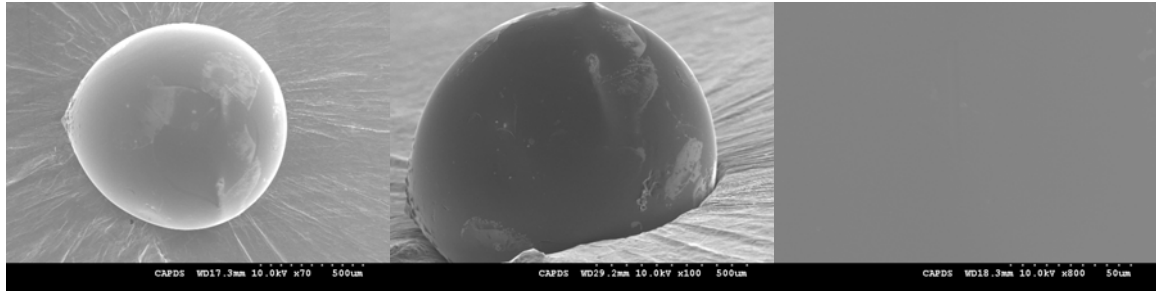
Silicon nitride is a very good insulating dielectric and it has been used widely in planar technology. Low temperature plasma deposited nitride has been proven to preserve good dielectric properties while the deposition can be performed with low thermal budget [31].

A layer of silicon nitride is deposited using Plasma Enhanced Chemical Vapour Deposition (PECVD) after the bonding of spheres and before n⁺ film deposition. The deposition gases are controlled in a NH₃:SiH₄ ratio of 10:1. A deposition temperature of 300 °C and power of 25 W is used. This recipe along with a pressure of 150 mTorr was proven to give good dielectric quality [35]. However, such low pressure promotes more directional growth which is not preferable in this application. A conformal film is desired because the insulating layer should cover the whole sphere surface and the sphere to substrate interface, therefore a higher pressure of 700 mTorr is used to achieve this purpose. After the deposition, a manual hydrofluoric acid (HF) wipe is used to remove the nitride from the top surface of the sphere.

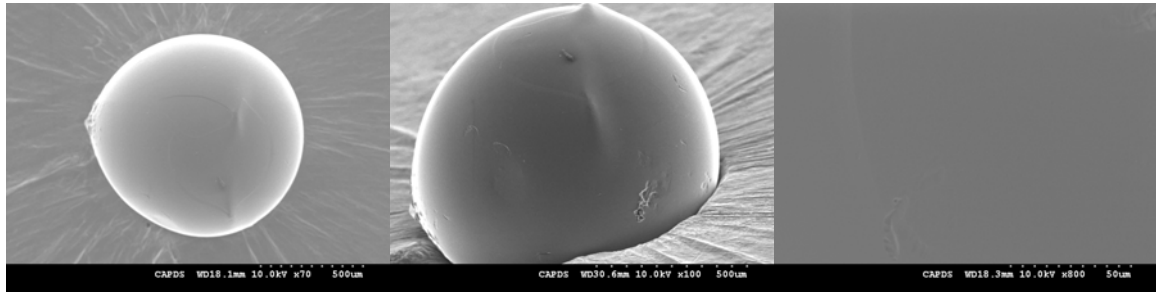
Although manual hydrofluoric acid wipe is an efficient method to remove nitride layer from the sphere surface, it is not a standardized step in process flow. First of all, since the sphere is so small,

HF would spread on along the sphere surface, reaching the interface between the sphere and the substrate. This case is similar to spin-on-glass discussed in section 4.5.1. Although the deposition of nitride is assumed to be conformal, it is still possible to get a thinner layer of nitride on the surface of the lower hemisphere because of the self-masking effect. In this case, concentrated HF in vapour phase can etch the thin insulating layer, ruining the purpose of nitride deposition. Secondly, several strokes of wiping may not be sufficient to completely remove the dielectric from the surface. This hypothesis is confirmed by low forward current in the case of thick nitride of about 1 μm which will be discussed in section 5.1.6. Therefore, an alternative to effectively remove nitride completely from the surface is investigated.

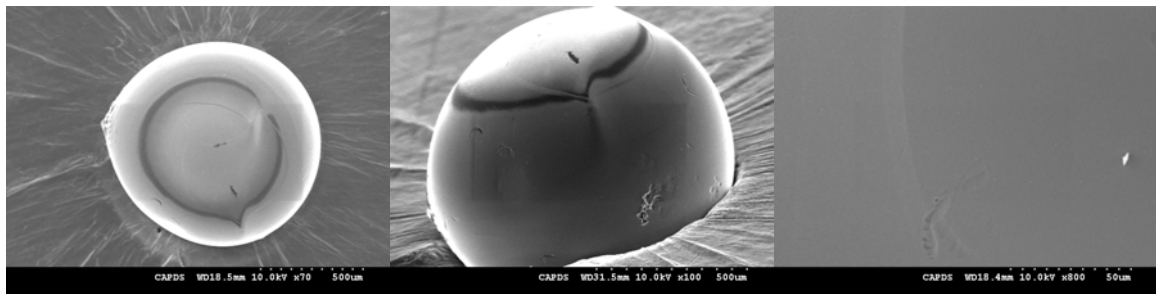
Reactive Ion Etching (RIE) has been developed as a technique for dry etching. This technique can be applied to the new structure due to the nature of anisotropic etching. Since the etching is directional, the nitride at the upper hemisphere would be removed while the nitride at the lower hemisphere would be shielded from reactive ions. The nitride is etched with the following process parameters, gas flow CF_4 of 17 sccm, H_2 of 3 sccm, pressure of 10 mTorr and DC bias of 500 V. The combination of low pressure and high bias provides the basis for anisotropic etching. A series of SEM images were taken to demonstrate the etching result in Figure 4.9. Instead of placing the sample directly in the RIE chamber, a shadow mask is used to expose the desired area for etching. This ensures the etching only take place at the upper hemisphere of the sphere. After the RIE process, the exposed silicon surface can be clearly identified from the high energy bombardment of the reactive ions in Figure 4.9 (c), suggesting etching of nitride has taken place in the RIE process.



(a)



(b)



(c)

Figure 4.9. SEM images of a sphere before and after the nitride deposition and RIE process. (a) bare sphere before nitride deposition (b) after nitride deposition (c) after RIE. Left: top view ($\times 70$), middle: side view ($\times 100$), right: magnified surface ($\times 800$)

To examine the directionality of the recipe, planar wafers posted at different angles were placed in RIE chamber for etching. The planar wafers were pre-deposited with 400 nm of silicon nitride. The angles of 0° , 45° , 90° and 135° were selected. With 300 seconds of etching, the nitride had almost been completely removed from the flat wafer as a shiny silver surface was revealed. The wafer posted at 45° resumed a shiny surface as well, although there was some nitride residue left along the edge due to edging effect. The wafer placed parallel to the direction of the ion beam gave expected result. The nitride at the upper part of the wafer was removed, while the nitride at the lower part was shielded from the etching. Thus it can be concluded that the nitride at the side

wall of the sphere could still survive after heavy etching. For the wafer with the side of nitride facing the bottom electrode at a 45° elevation, the colour of the nitride did not change, implying no etching took place when the nitride was shielded from the ion flux.

However, there are some concerns associated with RIE. First, the thickness of the nitride may vary across the sphere surface. Secondly, the etch rate would not be the same across the whole sphere surface due to anisotropic etching. As a result, some overetching may be required to completely etch away the nitride from the upper hemisphere. In addition, the etch rate for sphere would be different from the etch rate for a planar wafer, thus it is hard to control the etching time using planar wafer as calibration. To ensure that nitride is completely removed, overetching is unavoidable but it may negatively impact the performance of the device. High energy ion bombardment can damage the surface of the sphere, where the interface quality is critical in the performance of the junction. An overetch has been carried out in planar wafer to study its effect. After some excessive ion bombardment, the shiny silver surface becomes dull and black, implying the surface is textured. To further examine the roughness of the surface, profiler is used to look at the surface profile. Roughness of as large as 100 nm was measured. This roughness is even larger than the thickness of the film which is usually 50 nm. This poses an issue in anisotropic deposition as the film has poor coverage of uneven surface. Therefore, it is compulsory to avoid excessive overetching during RIE process. From the magnified image in Figure 4.10, some white dots are present at the sphere surface after RIE etching. These white dots were not observed in bare surface or the surface with nitride deposition. It is suspected that those are the damages from the ion bombardment. Although the bombardment impact on the device performance has not been investigated, the high energy ions introduce some damages to the surface morphology which may directly affect interface quality. However, if RIE is under well control, it can serve similar purpose as HF wipe.

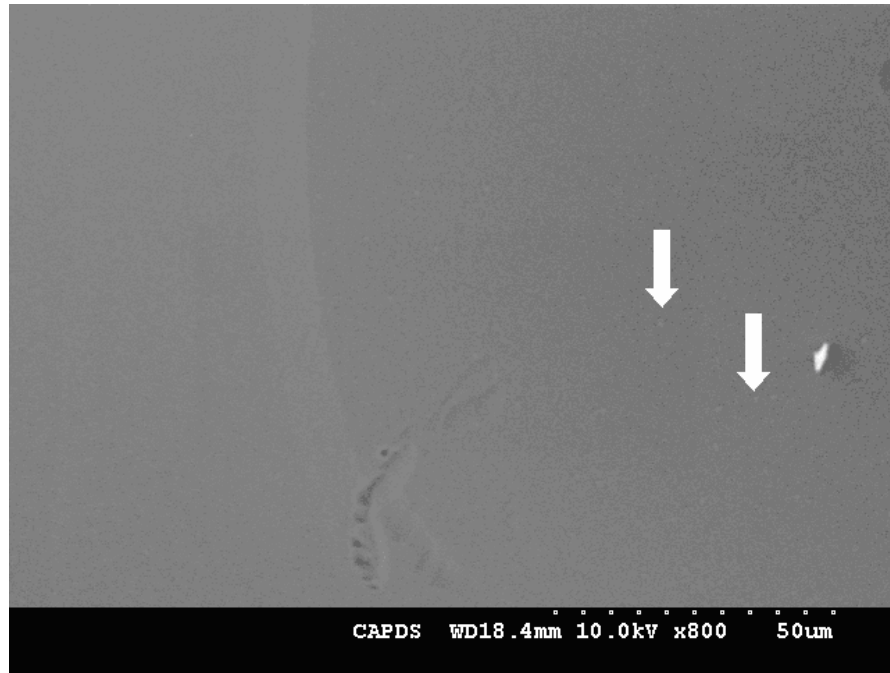


Figure 4.10. A close up image of the sphere surface after RIE with $\times 800$ magnification. Some white dots pointed by arrows are found in the image.

4.6 Summary

In this chapter, a new process flow has been tailored specifically for spherical silicon diode fabrication. The low temperature epitaxial film used in previous literatures is introduced and a discussion of applying the film on spherical structure has been initiated. Because of non-planar deposition surface, the deposited film will unlikely to preserve uniform thickness across the surface. This feature can be developed into a spherical diode without insulation layer by controlling the deposition parameters. To fully utilize the spherical surface for light absorption, insulation layer is required to isolate the continuous emitter layer from the substrate. Two schemes have been proposed and thoroughly evaluated. Spin-on-glass does not give a robust insulating layer due to various limitations. Silicon nitride has the potential to provide a good insulation layer but a technique of nitride removal from the sphere surface still needs to be developed. Using alumina can be another viable solution and further experiments should be designed and conducted.

Chapter 5

Junction Characterization of the New Spherical Device

In addition to the bulk quality, the junction quality plays an essential role in carrier collection.

At the p-n interface, the mismatch between two dissimilar materials can present additional dangling bonds and traps which further enhance the recombination process of the photogenerated carriers.

In this section, the dark current-voltage characteristic and capacitance-voltage characteristic are used to evaluate the quality of the junction.

5.1 Dark Current-Voltage Characteristic

Dark current-voltage (IV) characteristic is a simple tool to characterize junction quality and deduce electrical properties of solar cell [36]. Theoretically, the diffusion current in the quasi-neutral region follows an ideal exponential characteristic. However, non-ideal factors such as recombination and parasitic resistances distort the exponential behaviour and thus various models were derived to account for the deviation. A few influencing parameters, ideality factor, saturation current, parasitic shunt and series resistances can be extracted from the dark IV. Two popular models, one-diode and two-diode model, are widely used and are introduced here.

In one-diode model, only one linear region is identified in a logarithmic IV curve as shown in Figure 5.1. Beside the ideal region, non-idealities exist in low voltage and high voltage regions. For low current, the recombination in the depletion region dominates [36]. At moderate voltage, the current increases exponentially with a slope of e/mkT in logarithmic scale, where m is approaching 1 in the ideal case and e/kT is the inverse of thermal voltage. When the current is high, the performance of the diode is limited which is modeled by a series resistance. The current can be related to the voltage in the following relationship [36].

$$I = I_s \exp\left(\frac{e(V - I r_s)}{mkT}\right) \quad (5.1)$$

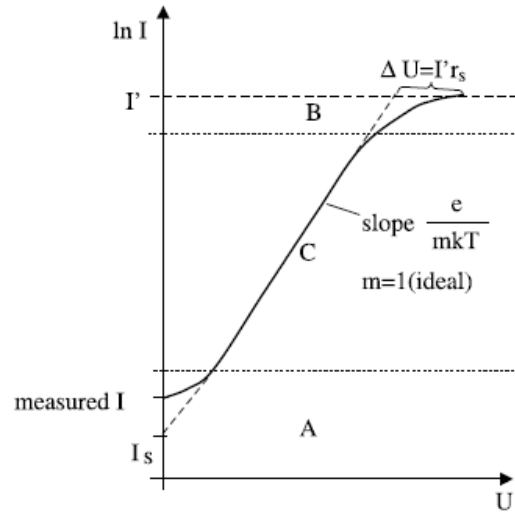


Figure 5.1. Current-voltage characteristic of a one-diode model in forward bias region in log scale [36]

One-diode model sometimes is not sufficient to describe the current-voltage characteristic. At low voltage, the current begins to deviate from the ideal exponential behaviour shown in Figure 5.2. Therefore, a two-diode model was derived to better describe the diode characteristic. For very low voltage, conductive path may exist which leads to a leakage current. This leakage current, only dominates at low voltage, can be modeled by a shunt resistance. At a slightly higher voltage of 0.2 V, exponential behaviour starts to prevail but the current grows at a slower rate compared to theoretical diffusion current, with a slope of $e/m_2 kT$. In this region, it was concluded that the recombination in the depletion layer dominates. The value of m_2 is approximately 2 assuming the recombination traps have an energy level right at the middle of the bandgap [36]. Beyond 0.4 V, the exponential relation slopes up at a higher rate of $e/m_1 kT$, exhibiting an ideal behaviour of diffusion current with m_1 approaching 1. The series resistance starts to introduce a negative effect at a higher voltage of 0.6 V and onward and the IV follows an ohmic characteristic. Combining all the parameters into a single equation, the dark current can be described as followed.

$$I = I_{ph} - I_{S1} \left(\exp \left(\frac{e(V - Ir_s)}{m_1 kT} \right) - 1 \right) - I_{S2} \left(\exp \left(\frac{e(V - Ir_s)}{m_2 kT} \right) - 1 \right) - \frac{V - Ir_s}{r_{sh}} \quad (5.2)$$

with I_{ph} as the photocurrent, I_{S1} and I_{S2} as the saturation current for the two diodes, m_1 and m_2 as the ideality factor for the two diodes, r_s as the series resistance and r_{sh} as the shunt resistance.

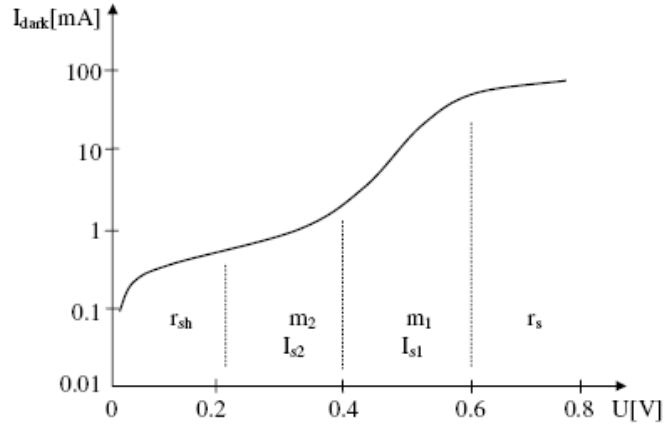


Figure 5.2. Current-voltage characteristic of a two-diode model in forward bias region in log scale [36]

5.1.1 Hydrogen Dilution

Figure 5.3 shows the current-voltage (IV) characteristic for different hydrogen dilution. The film thickness was estimated to be 120 nm and 100 nm for 92% dilution and 99% dilution respectively. The thick emitter ensures that the deposition can cover the whole upper hemisphere surface. It is evident that 99% dilution film gives a higher current than the 92% dilution film with 3 orders of magnitude difference but the two IV curves look very similar in shape. Although 99% dilution film gives a much higher current, the deposition rate of 2 nm/min is much slower than 92% dilution at a rate of 5.5 nm/min. Also high hydrogen dilution growth requires high deposition pressure, which is not a desirable feature as outlined in section 4.4.1 regarding the directionality. Upon the light illumination, 99% dilution film does not give a rise in open circuit voltage. On the other hand 92% dilution shows a slight shift to the right in the log scale IV curve. Demonstration of light illumination effect has made 92% dilution films the choice of n+ emitter in the subsequent experiments.

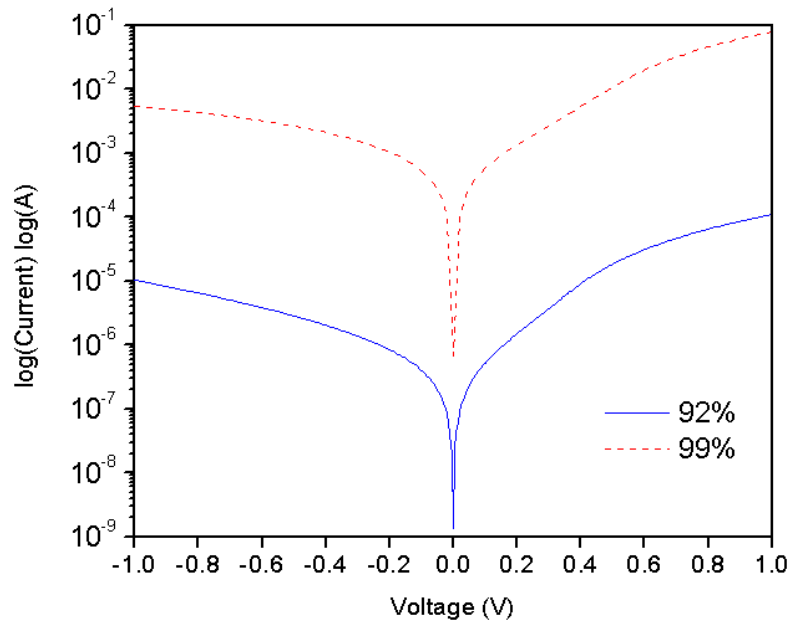


Figure 5.3. IV curve of emitter film with 99% and 92% dilution

5.1.2 Effect of Pressure

To promote directionality, the deposition pressure in the chamber should be lowered. As the pressure reduces, the radicals would experience fewer collisions, therefore they can travel in a more directed path [37]. However, the drawback of decreasing deposition pressure is that the deposition rate is significantly reduced. Since solar cell is a large area technology, the deposition rate should be high to ensure high throughput. To compensate the decrease in deposition rate, power can be varied to achieve higher deposition rate but to maintain film quality at the same time. Instead of using a pressure of 400 mTorr, the pressure is reduced to 200 mTorr to have directional deposition. An even lower pressure of 100 mTorr was attempted but the deposition did not give a visible colour change of the spheres and the substrate suggesting no film was successfully deposited. With a lower pressure, the deposition rate is lower but the relationship between pressure and deposition rate is not examined. It is assumed that the deposition rate decreases linearly with pressure.

5.1.3 Effect of Power

In order to maintain a reasonable deposition rate, a higher power should be used. There are some advantages for using higher power. A higher deposition rate is achieved since more dissociations occur from more energetic collisions between electrons and molecules. From energetic ion bombardment, the energy is transferred to the substrate thus can temporarily increase the surface temperature of the substrate [38]. With a higher surface temperature, crystallinity of the film can be improved because the radicals would be able to find a more energy favourable site. However, the power cannot be increased indefinitely. Although high energy ion bombardment can increase substrate surface temperature, it can introduce damage to the interface and the film degrading the film structure if the ion energy is too high. Also powder formation occurs because the secondary process is more likely to take place at higher power. To simplify the notation, the unit W is used for power and it is also equivalent to mW/cm^2 in terms of power density.

In this experiment, power of 60 W, 90 W and 120 W are studied with other deposition parameters remain constant. The following condition was used, temperature of 300°C , pressure of 200 mTorr, gas flow H_2 of 275 sccm, SiH_4 of 25 sccm, PH_3 of 10 sccm, deposition time of 15 minutes. The result is found in Figure 5.4.

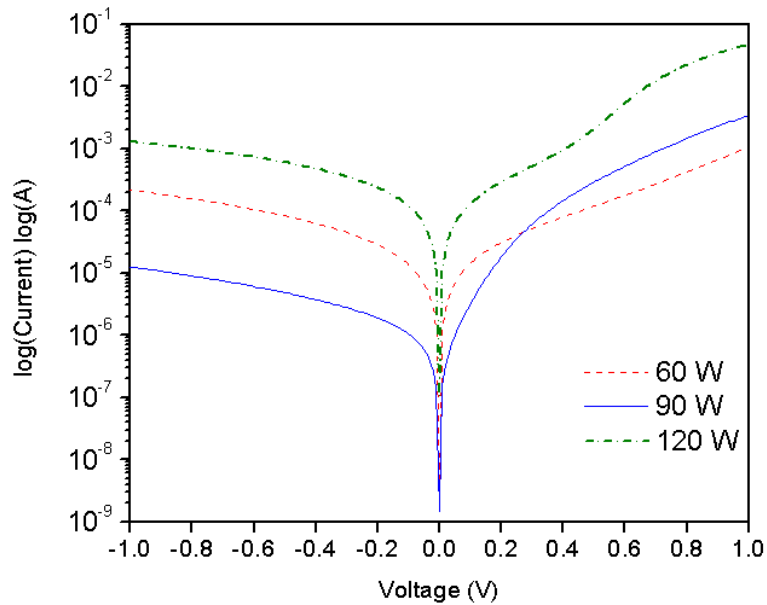


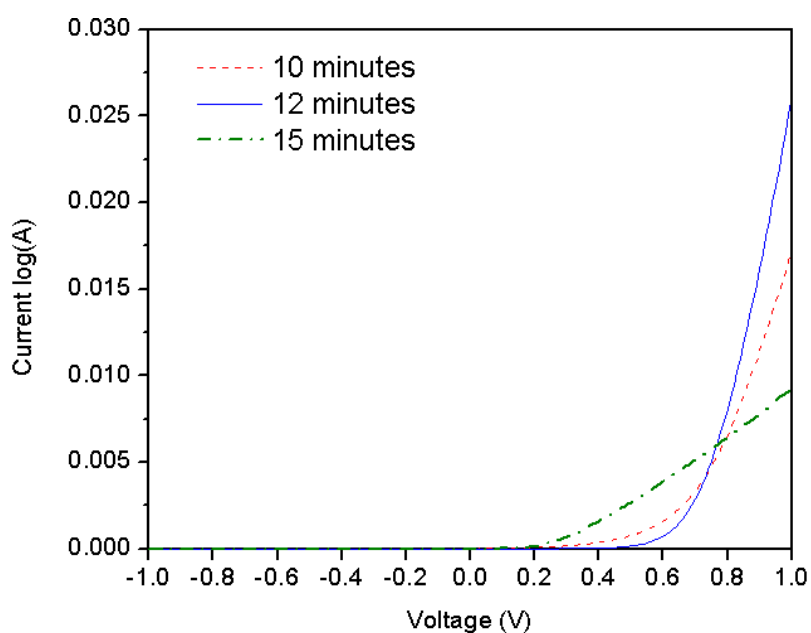
Figure 5.4. IV curve of 92% diluted film with constant pressure of 200 mTorr and 15 minutes of deposition in log scale

One of the performance metrics of diode application is to maintain low reverse current. From Figure 5.4, 90 W deposition has the lowest reverse current and gives a forward to reverse current ratio of about 100. In 60 W deposition, both the forward and reverse current are of similar magnitude, showing an apparent resistive characteristic. 120 W deposition results in a higher forward current but at the same time the reverse current increases to milliamp range. From the analysis, using power of 90 W is the most appealing choice and the combination of 200 mTorr pressure and 90 W power will be the focus of the study. In this experiment, the thickness of the films is not constant due to the fact that higher power yields faster deposition for fixed deposition duration. Although the thickness is not constant, it gives a rough idea on the effect of varying power.

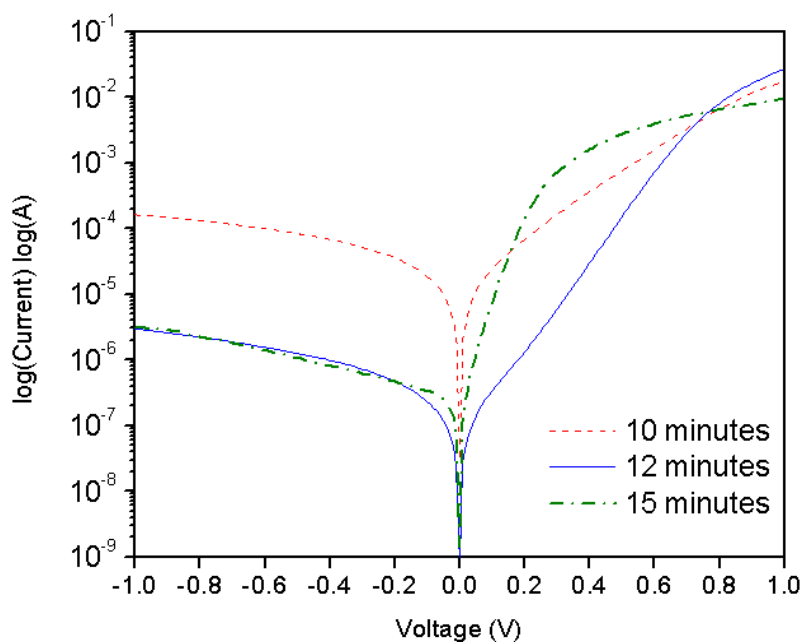
5.1.4 Effect of Deposition Time

As discussed in section 4.4.2, the thickness of the n⁺ emitter layer is crucial in solar cell performance. However, a method of measuring the thickness of the n⁺ layer on sphere has not been derived yet. Thus, the deposition time is varied to control the thickness of the film. The

deposition time of 12 minutes has been used exclusively in this research. The deposition time of 15 minutes and 10 minutes are used to see the effect of increasing and decreasing the thickness of the film, assuming the thickness is proportional to the deposition time. The IV characteristics are graphed in Figure 5.5.



(a)



(b)

Figure 5.5. IV curve of 92% diluted film with pressure of 200 mTorr, power of 90 W and varying deposition time in (a) linear scale (b) log scale

For a thinner emitter layer, it should give a higher forward current and lower reverse current theoretically but both phenomena are not observed. Out of five samples, only two of them give exponential curves as shown above. The other spheres have very low current in the forward bias region. It is possible that a bad contact is formed with the emitter layer and shorting happens under the metal layer. Interestingly, measuring the current outside of the contact pad gives better observable diode characteristic, implying highly conductive emitter layer is formed and the use of conductive oxide may be eliminated. A highly conductive nanocrystalline thin film has been found in [39]. All these hypotheses require further verification. At the reverse bias, there is no plausible explanation for the high reverse current.

A thicker film does not perform well in high voltage regime. The current rises exponentially in low voltage but it becomes linear too early, implying the current is limited in the device.

Space-charged limited current is one of the mechanisms causing the current to be limited in high electric field [40] but the voltage is too low for this to happen. In Figure 5.5 (a) with IV in linear scale, the current has a linear relationship with the voltage. This observation does not correspond to the fact that current has a parabolic relationship with voltage in space-charged limited current. A reasonable conclusion is that the series resistance is so severe that its effect is prominent in current even in milliamp range.

From the observations above, deposition time of 12 minutes remains the optimum choice for the purpose of study.

5.1.5 Comparison with planar results

The newly developed recipe using low pressure and high power is tested on planar wafer.

Comparison with planar substrate can verify that these process parameters can still give high quality low temperature epitaxial film. In the original recipe, 400 mTorr of pressure and 60 W of

power are used while the pressure is 200 mTorr and power is 90 W in the optimized film for spherical geometry. In Figure 5.6, it can be seen that the two films give similar performance. Both diodes show a two-diode characteristic with an ideality factor of 1.25 and saturation current of 2 pA in 0.4 – 0.6 V regime. The reverse current is well below 100 nA. The short circuit current and open circuit voltage is 2 μ A and 415 mV respectively. These values are smaller compared to the performance of crystalline silicon wafer solar cell because the active emitter layer is covered by the metal contact completely in the experiment. The coherent results prove the new recipe can achieve similar performance as the original film.

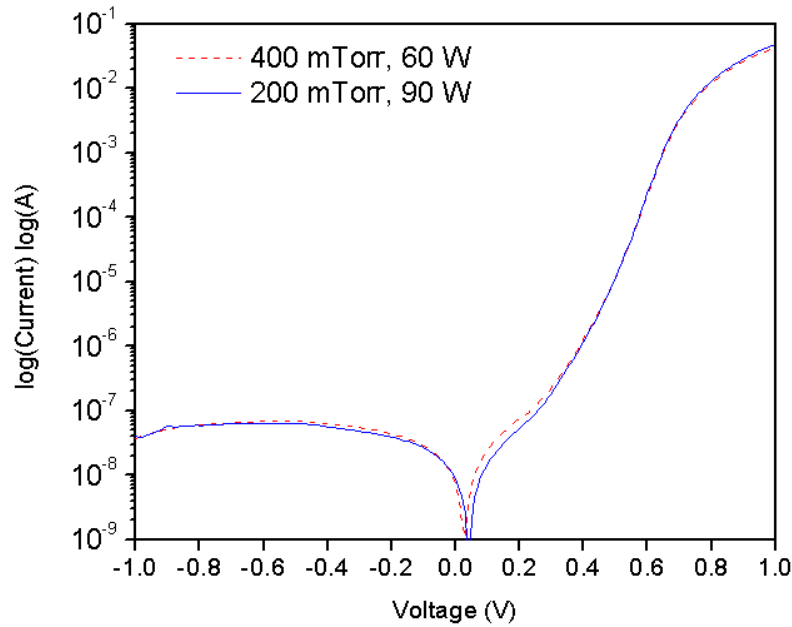


Figure 5.6. IV curve of original and newly developed film in log scale

The same film is deposited on the silicon sphere. The current-voltage characteristic however is inferior compared to the planar device, as evident in Figure 5.7. In the reverse bias, the reverse current goes up to 10^{-6} amps range and its magnitude increases when higher reverse voltage is applied. The increasing current in reverse voltage regime implies that there may be some conductive paths between the emitter film and the substrate. The slope of current increase in forward region is smaller compared to planar diode, suggesting a larger ideality factor for spherical

structure. Also, the recombination in the depletion region becomes less prominent when the ideal exponential comes in at a lower voltage. A double-diode characteristic is not clearly observed because the ideality factor in ideal exponential regime is so close to the ideality factor in lower voltage regime thus they merge together to give a single-diode characteristic. Although Figure 5.7 shows an IV characteristic measured without light illumination, planar wafer still give a certain open circuit voltage resulting from dim background light. On the other hand, spherical diode is much less sensitive to light seen from the fact that background light does not induce any open circuit voltage. Overall, the spherical diode performs worse than planar wafer in terms of leakage current suppression, ideality factor and light sensitivity.

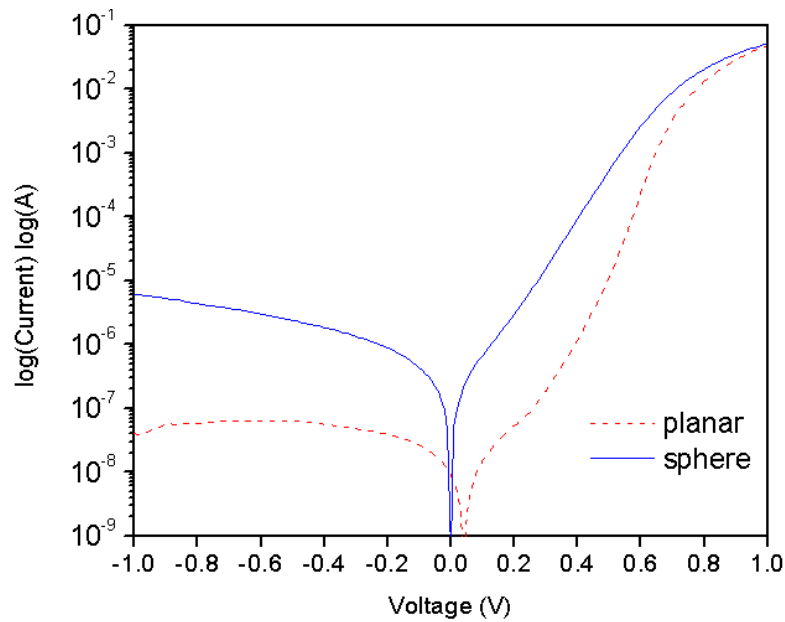


Figure 5.7. IV curve of 92% dilution epitaxial film with pressure 200 mTorr and power 90 W deposited on both planar wafer and sphere

5.1.6 Nitride as Insulating Layer

Because of the difficulty in measuring nitride film thickness on spherical structure, planar wafer is used to estimate the film thickness. For a 25-minute deposition, a 500 to 600 nm thick nitride film is formed on planar wafer. For a 50-minute deposition, the nitride thickness can reach 1 μm . It is assumed that 500 nm and 1 μm thick of nitride are deposited conformally over the sphere surface

for 25-minute and 50-minute deposition respectively. The nitride is removed from the top of the sphere using hydrofluoric acid wipe. Figure 5.8 and Figure 5.9 show the IV measurement with nitride as insulating layer for power of 90 W and 105 W respectively. It is shown that the best IV curve is achieved by 25-minute nitride deposition.

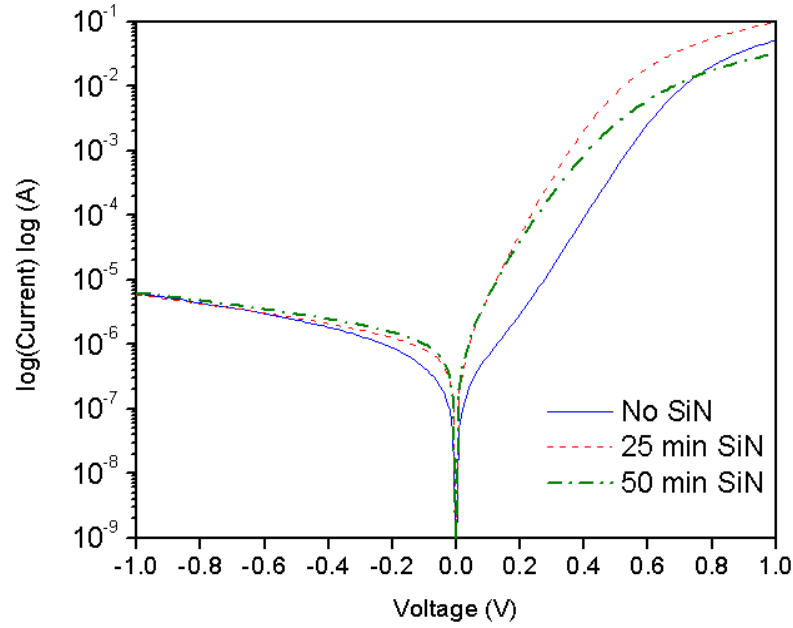


Figure 5.8. IV curve of 92% diluted film with 200 mTorr, power of 90 W and 12 minutes of deposition. The samples were pre-deposited with nitride of different thickness

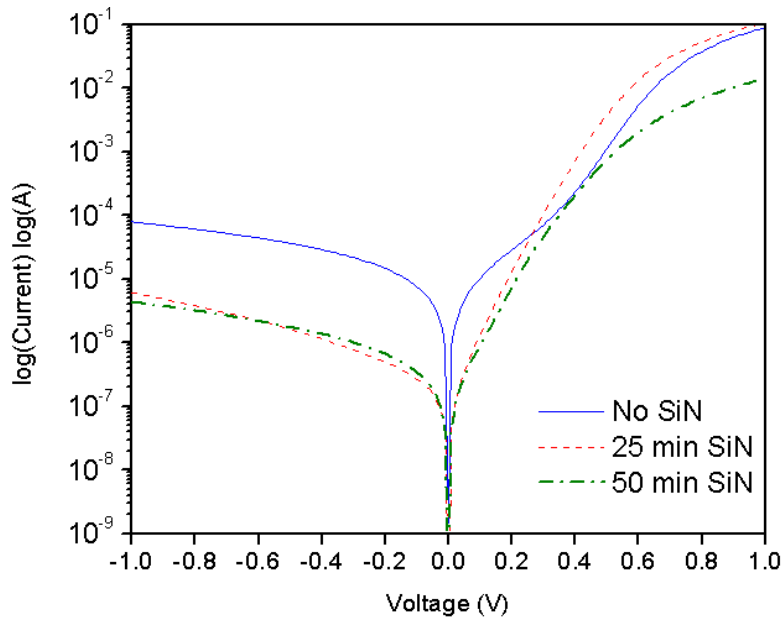


Figure 5.9. IV curve of 92%, diluted film with 200 mTorr, power of 105 W and 12 minutes of deposition. The samples were pre-deposited with nitride of different thickness

From the figures above, the effect of nitride in reverse current reduction is evident. The result is not apparent in the case of 90 W power deposition since the reverse current is low even without nitride deposition. In this case the deposition of nitride does not help in reduction of reverse current. For the film with 105 W deposition, the reverse current is high without insulation as expected because deposition with higher power results in a higher deposition rate. For the same deposition time, a thicker film would be formed, increasing the chance of providing more coverage of the sphere surface and possibly shorting the film to the substrate. The nitride deposition in this case has successfully reduced the reverse current by one order of magnitude.

Additionally, nitride has modified the current-voltage characteristic. Without nitride deposition, the curve demonstrates a two-diode characteristic. At moderate voltage of 0.4 – 0.6 V, the diffusion current dominates and exhibits an ideal exponential dependency on voltage. At low voltage, however, the current does not increase according to the ideal exponential but the increase is reduced by a factor of 2. The recombination current in the space charge region dominates as dangling bonds in the depletion layer exist as neutral traps [41]. With nitride deposition and hydrofluoric acid wiping, only one-diode approximation is observed from the characteristic. The result suggests that the recombination current in depletion region does not introduce a dominating factor at low voltage. The dangling bonds in the space charge region primarily come from the material itself and additional dangling bonds found at the interface between the p and n layer. For a spherical surface with non-epitaxial growth of emitter layer, the interface can be considerably defective because low temperature epitaxial growth does not encourage atoms to find energy favourable sites, leaving behind dangling bonds at the interface. With insulation deposition, silicon nitride serves the purpose of passivation of defects and dangling bonds at the surface. Before n+ layer deposition, hydrofluoric acid (HF) wipe is carried out to remove the nitride layer. The HF wipe may not be efficient so it is possible of having incomplete removal of nitride. The residual nitride can still passivate the dangling bonds, reducing the number of dangling bonds at the

p-n interface in consequence. The recombination in the depletion layer is thus minimized.

Another effect of incomplete nitride removal is low forward current. It is evident in the case of thick nitride deposition which the forward current is reduced by as much as 1 order of magnitude. For moderate nitride thickness of 500 nm, hydrofluoric acid wipe is likely to remove the nitride but nitride of 1 μm may not be easily removed by application of a few strokes of HF wiping. A layer of insulating nitride at the surface results in a p-i-n structure. The insulating layer, however, is so thin that most of the carriers can still tunnel through and the diffusion current still increase exponentially, but at a reduced rate.

Instead of using hydrofluoric acid wipe, Reactive Ion Etching (RIE) is performed to remove nitride. In RIE etching a shadow mask with 0.8 mm-diameter hole is used to define the surface to be etched thus the area of the device will be smaller in this case. The comparison is found in Figure 5.10. Emitter layer on sphere with RIE etching of silicon nitride gives diode characteristic but does not outperform HF wiping in forward bias. First of all, the process of RIE etching is not optimized. RIE etching rate on spherical surface is found to be slower than etching performing on planar wafer. Even though nitride film on sphere is RIE-etched for longer time, it is not possible to ensure that the nitride has been successfully removed. A side effect of RIE etching is the bombardment of the surface, resulting in deterioration of interface quality. Although the forward current is smaller, RIE etching of nitride is successful in keeping the reverse current at a lower level. The directional ion bombardment and shadow mask can make sure that the insulation layer at the side wall and lower hemisphere will not be removed.

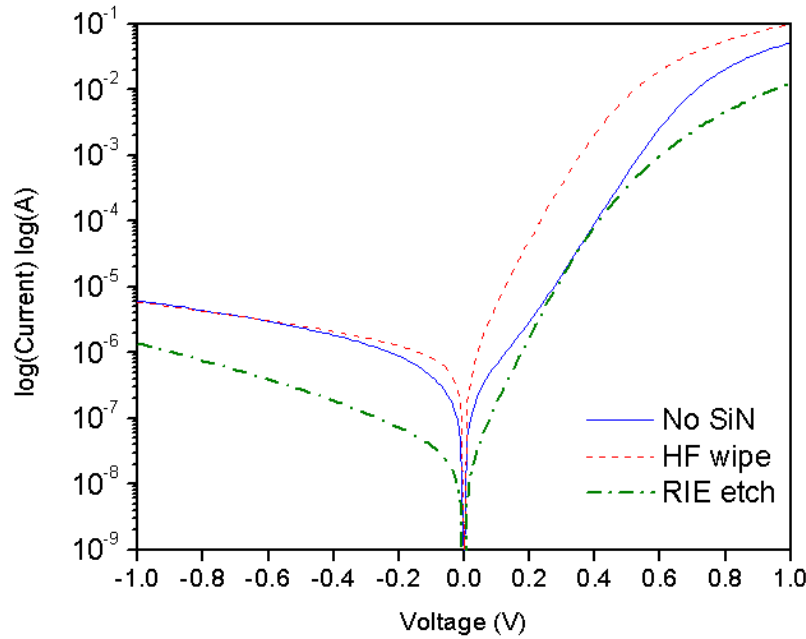


Figure 5.10. IV curve for 92%, diluted film with 200 mTorr, power of 90 W and 12 minutes of deposition. 25-minute nitride deposition was conducted prior emitter deposition. The nitride is removed by either hydrofluoric acid or reactive ion etching

5.2 Calculation of Parameters

A few essential parameters are calculated to fit the two-diode model presented in section 5.1. The ideality factor and saturation current give a direct relationship between voltage and current. The shunt and series resistances are the parasitic effects which model the non-ideality at extremely low voltage and high voltage regimes. These parameters give important insight on junction quality as well as diode performance relative to standard or other diodes.

5.2.1 Ideality Factor and Saturation Current

From the current-voltage characteristic, a few parameters can be extracted. In a two-diode model, the ideality factor n_1 and saturation current J_{S1} correspond to recombination resulting from Shockley-Read-Hall recombination traps in the bulk. In the depletion region, the recombination can be modeled by ideality factor n_2 and saturation current J_{S2} . A current-voltage curve of 92% of hydrogen dilution, 200 mTorr of pressure, 90 W of power, and 12 minutes of deposition time is shown in Figure 5.11.

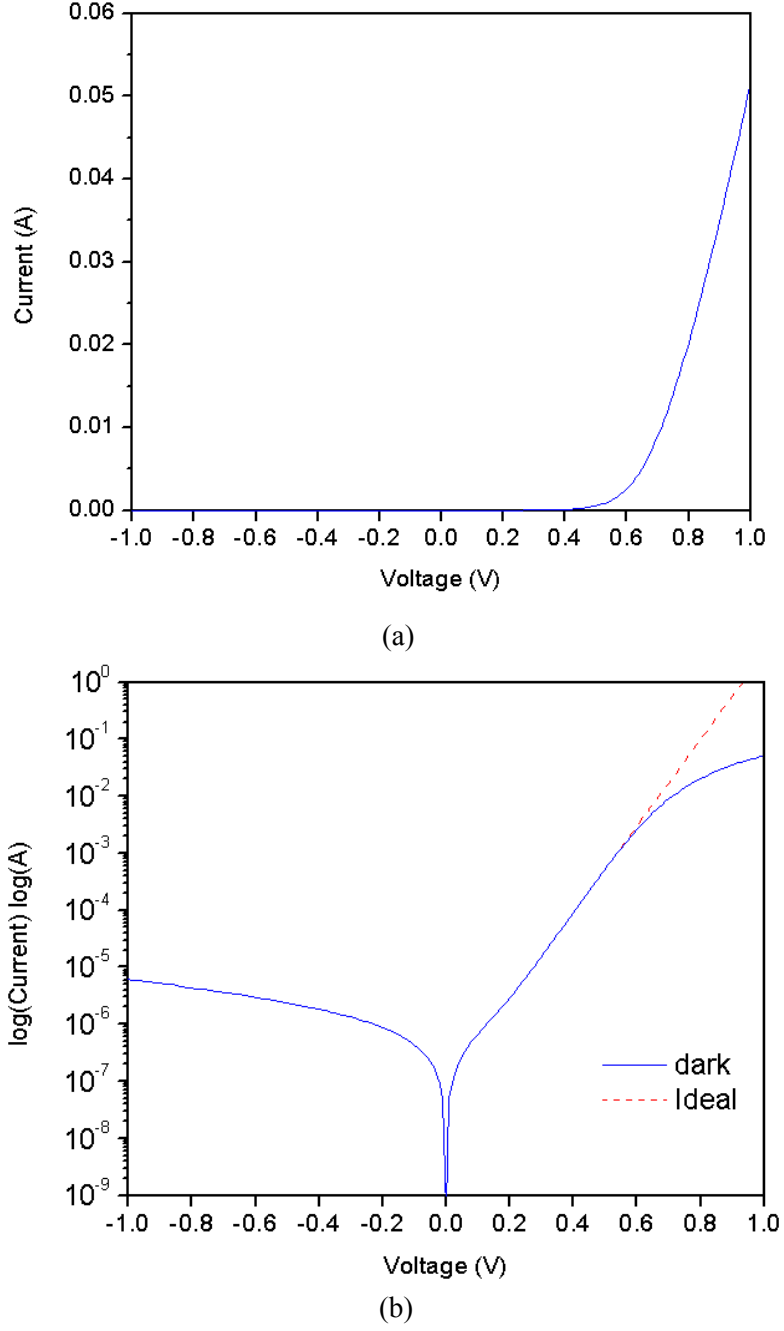


Figure 5.11. IV curve of 92%, 200 mTorr, 90W, 12 minutes (a) linear scale (b) log scale

From Figure 5.11 (b), it can be observed that the device behaves like a two-diode circuit. A curve fit was used to estimate the parameters from the measured data. From 0.15 V to 0.25 V, the exponential approximation of n_2 and J_{S2} is 2.5 and 1.36×10^{-7} A respectively. From 0.35 V to 0.55 V, it was identified as the ideal diode region. The exponential approximation of n_1 and J_{S1} is 2.2 and 8.17×10^{-8} A respectively. The ideality factor of $n = 2.2$ is quite far away from the theoretical ideal limit of 1.0 for crystalline silicon p-n junction. The high value of ideality factor is due to the

recombination loss in the bulk. The deviation from the ideal $n = 1$ can be attributed to various factors [42]. For a highly doped bulk, the ideality factor approaches a value of 1.5. With energy traps located at the midgap, $n = 1.8$ can be easily obtained. For the spheres used in the experiment, the low quality bulk introduces severe recombination which dominates over diffusion current even in moderate voltage. This factor is therefore the major contribution to high ideality factor of $n \approx 2$.

5.2.2 Shunt and Series Resistance

At very low voltage (smaller than 0.06 V), the current has a linear relationship versus voltage. This is clearly seen by the logarithmic curve between 0 V to 0.06 V in Figure 5.11 (b). This effect is translated into ohmic behaviour in linear scale, known as shunt resistance. By curve fitting, shunt resistance is estimated to be $1.8 \times 10^5 \Omega$. This shunt resistance can be neglected in the higher voltage regime because its impact to the IV curve is insignificant. From voltage above 0.6 V, the curve commences to deviate from the exponential characteristic and demonstrates an ohmic behaviour. The desired value for series resistance should be less than 0.5Ω [36]. Estimated from the curve, series resistance is found to be 4.5Ω , which is ten times larger than the ideal value, causing the current to drop drastically above 0.6 V.

5.3 Capacitance-Voltage Characteristic

A capacitance-voltage (CV) characteristic contains important information including built-in voltage. When a p-type semiconductor comes in contact with an n-type semiconductor, the free carriers on each side diffuse across the junction due to carrier concentration gradient, leaving immobile ions behind [43]. The diffusion process stops when the immobile ions create a large enough electric field in the transition region. The space charge region where free carriers are depleted can be treated as dielectric. Free charged carriers at the edge of the space charge region with no carriers exist in between forms a parallel plate capacitance. This capacitance is known as junction capacitance defined as

$$C = \left| \frac{dQ}{dV} \right| \quad (5.3)$$

with Q being the charge in the depletion region and V being the voltage across the region. The junction capacitance for a p-n junction is thus

$$C_j = \frac{\varepsilon A}{W} = A \sqrt{\frac{e \varepsilon_s}{2(V_{bi} + V_r)} \frac{N_D N_A}{N_D + N_A}} \quad (5.4)$$

where C_j is the junction capacitance, A is the area of the diode, W is the depletion width, e is the electron charge, ε_s is the permittivity of silicon, V_{bi} and V_r are the built-in voltage and reverse voltage respectively, N_D and N_A are the carrier concentration of n-side and p-side. With applied voltage, the width of depletion layer changes causing a variation in capacitance. At reverse bias, the space charge region width increases, therefore the junction capacitance decreases according to Equation (5.4). For an n⁺-p diode, the doping level N_D is much larger than N_A , thus the expression can be simplified to

$$C_{junction} = A \sqrt{\frac{e \varepsilon_s N_A}{2(V_{bi} + V_r)}} \quad (5.3)$$

This expression is valid for one-side abrupt junction only. The junction with low temperature epitaxial film can be classified as one-side junction because the emitter is heavily doped so the depletion layer extends mostly in the p-type bulk. It is an abrupt junction with uniform doping on both n⁺ and p side. It is also a convention to plot the $1/C^2$ graph because of its linear dependency with voltage.

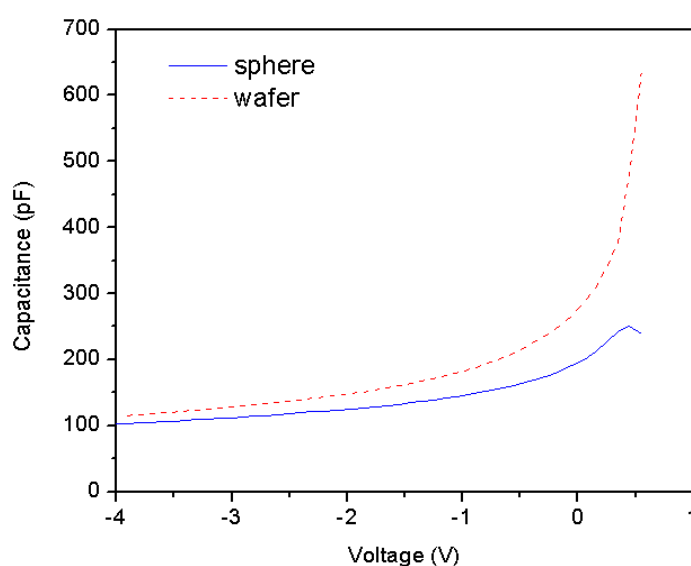
$$\frac{1}{C^2} = \frac{2(V_{bi} + V_r)}{e \varepsilon_s N_A A^2} \quad (5.4)$$

From this relationship, the built-in voltage can be determined when the left hand side of Equation (5.4) is set at zero. The slope of the straight line can be used to deduce doping concentration.

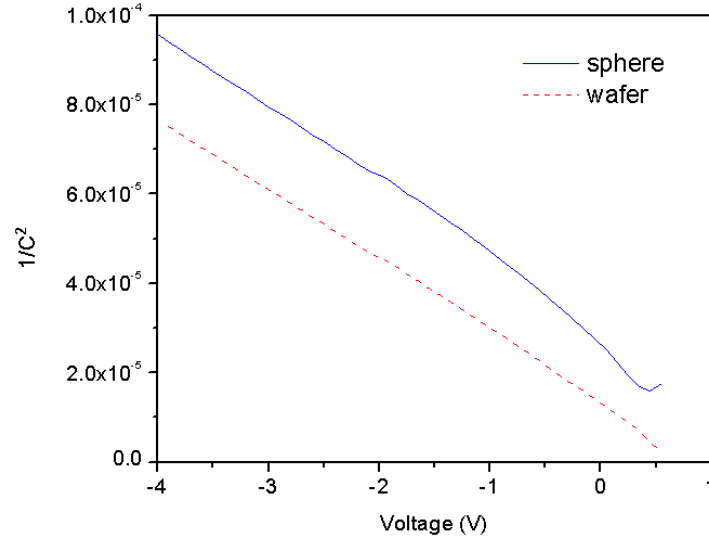
5.3.1 Built-in Voltage

In order to measure the capacitance of the diode properly, the emitter film is etched away first by Reactive Ion Etching (RIE). Only the emitter underneath the aluminum contact survives. Before the dry etching, the actual area which the emitter film cover the sphere could not be accurately predicted. The etching would ensure a defined area diode is created.

The CV and $1/C^2$ curves in Figure 5.12 demonstrate capacitance-voltage characteristic for both planar wafer and sphere. The emitter film is deposited with a power of 90 W for 12 minutes. For an appropriate capacitance voltage characteristic, it should follow a linear relationship in $1/C^2$ plot for abrupt junction, which is proven in Figure 5.12 (b). The magnitude of the capacitance should not be emphasized on because the area of the diodes is different. In planar diode, it follows the linear relationship of $1/C^2$ versus voltage very well, suggesting the deposited emitter film forms an excellent abrupt junction with crystalline silicon. Spherical diode follows similar trend at high reverse bias. This ideality however is not preserved for voltage less than -1 V. This observation is similar to the amorphous/crystalline silicon heterojunction which will be discussed in section 5.4.



(a)



(b)

Figure 5.12. Capacitance-voltage characteristic of low temperature epitaxial emitter on sphere and wafer. The graph is plotted in (a) linear scale, (b) $1/C^2$ versus voltage

By inspecting $1/C^2$ curve, one can extract the built-in voltage by extrapolating the linear region to intercept with the voltage axis. The measurement is repeated for a few spheres on the same substrate. By performing the extrapolation, the built-in voltage for junction without nitride ranges from 0.93 V to 1.85 V and the built-in voltage for junction with insulation ranges from 0.71 V to 0.87 V. For a homogeneous junction, the built-in voltage depends on the doping in the following way.

$$V_{bi} = \frac{kT}{e} \ln \left(\frac{N_A N_D}{n_i^2} \right) \quad (5.5)$$

where n_i is the intrinsic carrier concentration in silicon. For an n+-p homogeneous diode, the built-in voltage is about 0.8 V. In heterogeneous junction, this calculation would not be valid. In the case of amorphous/crystalline silicon heterojunction, the built-in voltage can be higher due to larger bandgap in amorphous silicon [44]. For amorphous silicon p-i-n junction the built-in voltage can be as high as 1.2 V [45]. From the curve above, the extrapolated built-in voltage is greater than 1 V, which is outside of the anticipated value. Looking at the diodes with silicon

nitride as insulating layer, the average V_{bi} value is found to be 0.81 V. The extrapolated result of 0.8 V appears to be a plausible result because low temperature epitaxial film may have a larger bandgap due to existence of amorphous phase. Nonetheless, the capacitance-voltage measurement confirms a junction formed with the low temperature epitaxial silicon film demonstrating diode characteristic.

5.4 Comparison with other Heterojunctions

At this point, the junction quality of a low-temperature deposited film on sphere has not been microscopically characterized. A direct characterization of the interface and film quality using Transmission Electron Microscope (TEM) has not been performed due to technical issue but indirect methods such as comparing current-voltage and capacitance-voltage characteristics with well-characterized junctions can be used. The spherical diode will be compared with (a) amorphous/crystalline silicon (a-Si / c-Si) heterojunction [44] and (b) quasi-epitaxial crystalline/multicrystalline heterojunction (qEpi-Si / mc-Si) [39]. The diodes above are compared with the low temperature deposited film developed in this thesis on crystalline silicon substrate in (c) spherical geometry and (d) planar geometry. The heterojunction (a) has a heavily doped n⁺ amorphous film of 20 nm deposited on top of crystalline silicon with an ultra thin intrinsic amorphous film of 5 nm in between. Junction (b) has a n⁺ quasi-epitaxial crystalline film of 50 nm deposited on top of multicrystalline silicon substrate.

5.4.1 Current-Voltage Characteristic

Figure 5.13 shows the current-voltage characteristics of the four different diodes. The currents are not normalized by the area as data from other sources are not available. By looking at the shape of the IV curve, it is sufficient to make some important conclusions regarding the quality of the diode. The spherical diode IV characteristic performs very similar to the a-Si / c-Si diode. Both of them have same magnitude of reverse current and similar slope in the forward bias diffusion current

region. This fact suggests that the deposited film on sphere tends to be amorphous. The same film deposited on crystalline silicon, however, has similar characteristic compared to quasi-epitaxial film deposited on multicrystalline substrate. Both devices have similar degree of reverse current and forward current although the newly developed film does not perform as well as the quasi-epitaxial film developed in [39]. Since both of them possess similar characteristic, the film developed in this thesis can still be classified as quasi-epitaxial with high crystallinity. The same film deposited on silicon sphere however gives similar characteristics as the amorphous film, implying low crystallinity on spherical geometry. An essence in quasi-epitaxial film is that the substrate should be single crystalline so the deposition can clone the crystal structure. Although the sphere is quoted as single crystalline, the arriving radicals may not see “single crystalline” during the deposition. Experimental results have shown that the same deposition condition on a (111) oriented wafer results in amorphous growth [46]. At a deposition condition of 200 °C, a crystalline film can be formed on a wafer of (100) for 30 nm, but at the same temperature the film appears to be amorphous grown on a (111) wafer. Because of the non-planar geometry, the incoming atoms arriving at an angle to the surface can see different orientation than (100) during the plasma deposition. Consequently, the deposited film on non-planar geometry can have more amorphous content than crystalline structure.

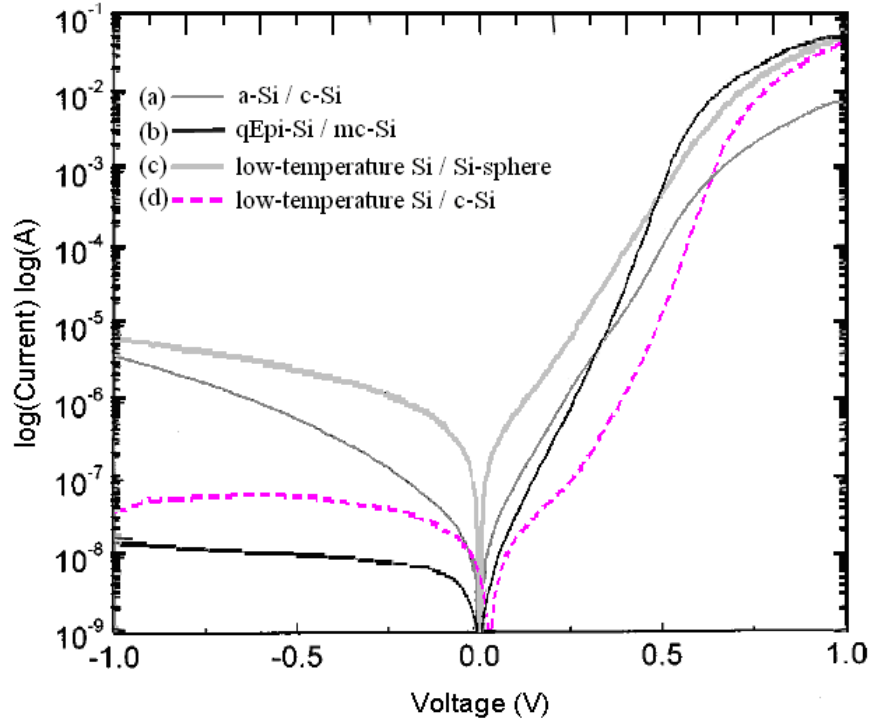


Figure 5.13. IV curve of the heterojunction diodes. (a) amorphous on crystalline silicon (0.03 mm^2) (b) quasi-epitaxial silicon on multicrystalline silicon (2.25 mm^2) (c) low-temperature film on sphere (0.3 mm^2) (d) low-temperature film on crystalline silicon (1 mm^2) [32, 44]

5.4.2 Capacitance-Voltage Characteristic

Figure 5.14 shows the capacitance-voltage characteristics of the above diodes. Once again the capacitance value is not normalized. The CV results converge with the conclusions drawn in the observation of dark IV characteristic. Both (b) and (d) demonstrates abrupt junction characteristic. The V_{bi} in (b) is 720 mV as mentioned in [39] and the V_{bi} valued at an average of 810 mV for the newly developed film deposited on planar crystalline substrate. Comparing (a) and (c), both of them show non-ideality at low reverse bias. An explanation of this non-ideality stems from interface states presenting traps in the bandgap [47]. For amorphous silicon, the low bias CV is affected by the defective band tail states. In the case of deposited film on sphere, the interface defects can be high enough to degrade the CV characteristic, and/or amorphous film is deposited instead of highly crystalline film. The contributions from these two effects cannot be clearly identified without direct examination of film quality.

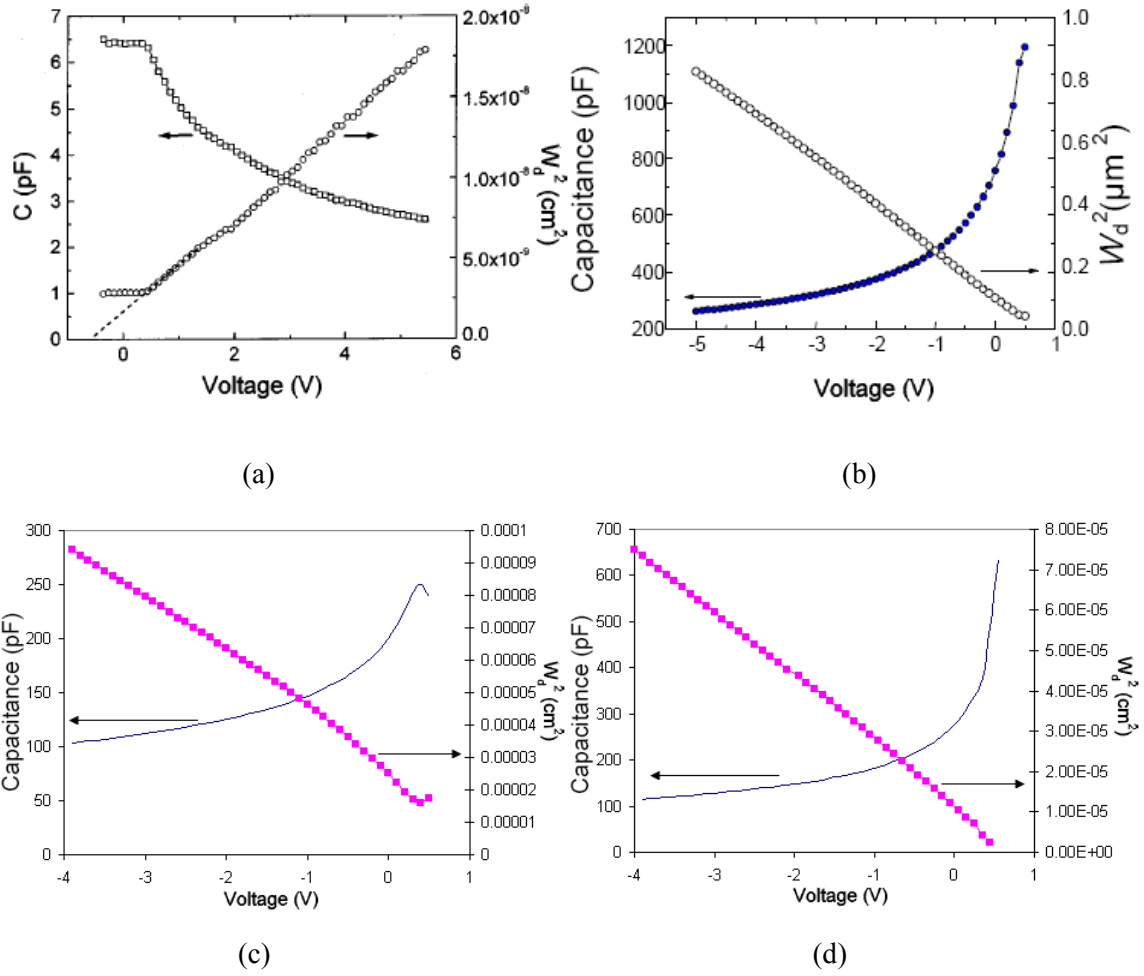


Figure 5.14. CV curve of the heterojunction diodes. (a) amorphous on crystalline silicon (0.03 mm^2) (b) quasi-epitaxial silicon on multicrystalline silicon (2.25 mm^2) (c) low-temperature film on sphere (0.3 mm^2) (d) low-temperature film on crystalline silicon (1 mm^2) [39, 44]

5.5 Summary

Both the current-voltage and capacitance-voltage relationship of spherical diode show legitimate p-n diode characteristic. For spherical device, a low temperature epitaxial film with low pressure and high power is developed. This highly directional film allows the absence of insulating layer between deposited emitter and conductive substrate. The use of insulating layer is also studied. The insulating layer can reduce the reverse current by an order of magnitude compared to device without insulation. Regarding the removal of nitride layer, both hydrofluoric acid wipe and reactive ion etching can perform the task but reactive ion etching has the chance to induce damages to the sphere surface, degrading the interface at the junction. The low temperature epitaxial film

with low pressure and high power developed for sphere was deposited on planar wafer. The current-voltage characteristic reveals superior performance similar to the original emitter recipe with moderate pressure and power. The performance of the low temperature epitaxial film on spherical silicon, however, is inferior compared to the planar device of similar structure. From the IV characteristic, spherical diode demonstrates high ideality factor of 2.2 and high saturation current. In the reverse bias, the diode also fails to keep the reverse current below 100 nA. From the capacitance-voltage characteristic, its result is very similar to amorphous/single crystalline silicon diode, implying the low temperature deposited film on spheres has low crystallinity.

Chapter 6

Photovoltaic Characteristic under Illumination

To fully characterize a photovoltaic device, diode characteristic under illumination should be carefully studied. The shape of the illuminated current-voltage curve provides valuable information on short circuit current (I_{sc}), open circuit voltage (V_{oc}) and fill factor (FF). Short circuit current and open circuit voltage define the theoretical limit of device performance. To extract quantum efficiency, spectral response measurement is conducted to assess the effectiveness of carrier generation and collection for specific wavelength. These characterization techniques give insight on the limiting factors in performance so further improvement can be designed for future development.

6.1 Illuminated Current-Voltage Characteristic

The current-voltage measurement was taken with the spheres illuminated under a strong lamp with intensity of 10,000 foot-candles [48]. Unfortunately, a strong response of short circuit current was not observed. It does, however, give a higher current under illumination as shown in Figure 6.1 (a), evident from the fact that the short circuit current is 3 orders magnitude larger than the dark current. This extremely low short circuit current, valued at 300 nA, is 3 orders smaller than the nominal short circuit current reported in literatures [28]. If 200 μ A of short circuit current is applied to the curve, the open circuit voltage can reach 450 mV as shown in Figure 6.1 (b), which is closer to the theoretical value. It can be concluded that the main contribution of low open circuit voltage and fill factor comes from the exceptionally low short circuit current of the device.

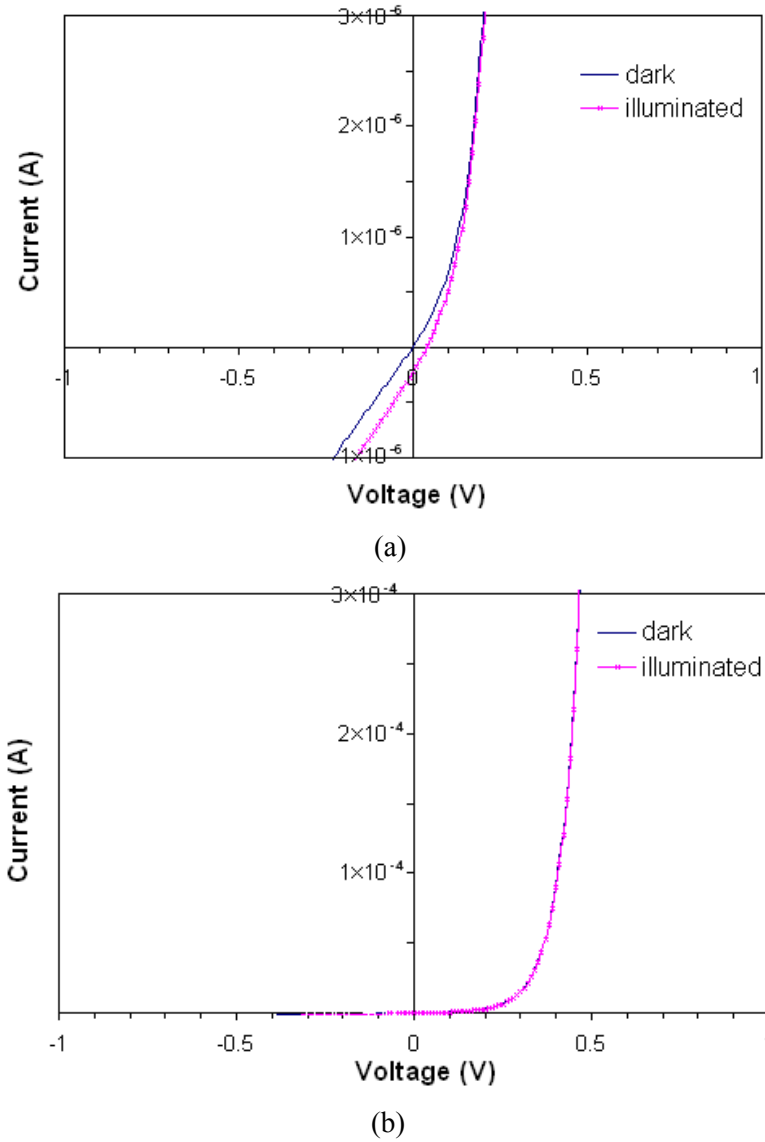


Figure 6.1. Dark and illuminated IV curve of 92% diluted film with 200 mTorr, 90 W and 12 minutes of deposition. Current ranges from (a) $-1 \mu\text{A}$ to $3 \mu\text{A}$ (b) 0 to 0.3 mA

6.2 Short Circuit Current and Open Circuit Voltage

From experimental results, the short circuit current for spherical diode remains unreasonably low, in the range of $0.1 \mu\text{A}$. I_{SC} has a proportional relationship with the external quantum efficiency. The low quantum efficiency investigated in section 6.3 can be a plausible reason for low I_{SC} .

The open circuit voltage was not consistently measured. The high end value is about 130 mV, while for some devices no open circuit voltage is observed. The measured V_{OC} is much lower than 600 mV for planar diode. With a high built-in voltage (V_{bi}) measured by

capacitance-voltage characteristic, the theoretical open circuit voltage can be as high as 80% of V_{bi} [45]. A general expression of V_{OC} is

$$V_{oc} = \frac{nkT}{q} \ln \left(\frac{I_{sc}}{I_s} \right) \quad (6.1)$$

where I_s is the saturation current. Given a low I_{sc} , the saturation current must be extremely small to give an observable open circuit voltage. The saturation current is determined by

$$J_0 = J_{0e} + J_{0b} = \frac{qn_i^2 D_p}{L_p N_D} + \frac{qn_i^2 D_n}{L_n N_A} \quad (6.2)$$

where n_i is the intrinsic carrier concentration, D_p and D_n are the diffusion coefficients for electrons and holes, L_n and L_p are the diffusion lengths for electron and holes and N_D and N_A are the doping densities of the emitter and bulk. The saturation current has an inverse relationship with the diffusion length, which is very small in the sphere due to defective low quality bulk. With a lower measured lifetime, the open circuit voltage is smaller. This can be confirmed experimentally as indicated in Figure 6.2.

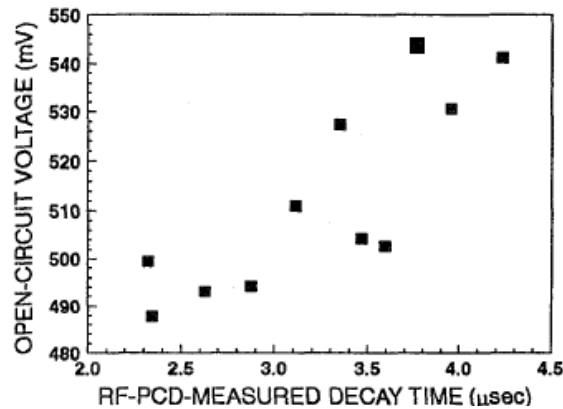


Figure 6.2. Open circuit voltage dependency on measured lifetime [20].

6.3 Spectral Response

Spectral response measures the external quantum efficiency of the photovoltaic cell as a function of wavelength. Quantum efficiency, which is defined as ratio of the number of photons collected at

the external circuit to the number of incident photons, is particularly important in calculating the short circuit current [49].

$$J_{sc} = q \int b_s(E) QE(E) dE \quad (6.4)$$

with J_{sc} as the short circuit current density, q as the charge of electron, $b_s(E)$ as the incoming spectral flux, $QE(E)$ as the external quantum efficiency and E as the energy of the incoming photons, which is inversely proportional to the wavelength. From the spectral response, it is possible to draw some conclusions on junction quality by comparing to some standard response.

6.3.1 Spectral Response of Diffused Emitter Cell

In traditional spherical technology, the n+ emitter is formed by phosphorous diffusion in the p-type sphere. A spherical photovoltaic module has been constructed using diffused emitter in previous work [29]. The 6" × 6" array consists of tiny p-n junction spheres with average radius of 390 μm. The spheres are first coated with titanium oxide (TiO₂) as the anti-reflection coating. Then they are thermomechanically bonded to a foil with perforated holes, making a contact with the n+ layer. The back of the spheres are etched to expose the bulk. With the application of an insulating layer and another foil, a back contact is made by bonding the p-type spheres to the back foil. This standard module has a peak quantum efficiency of 68% at 660 nm as demonstrated in Figure 6.3.

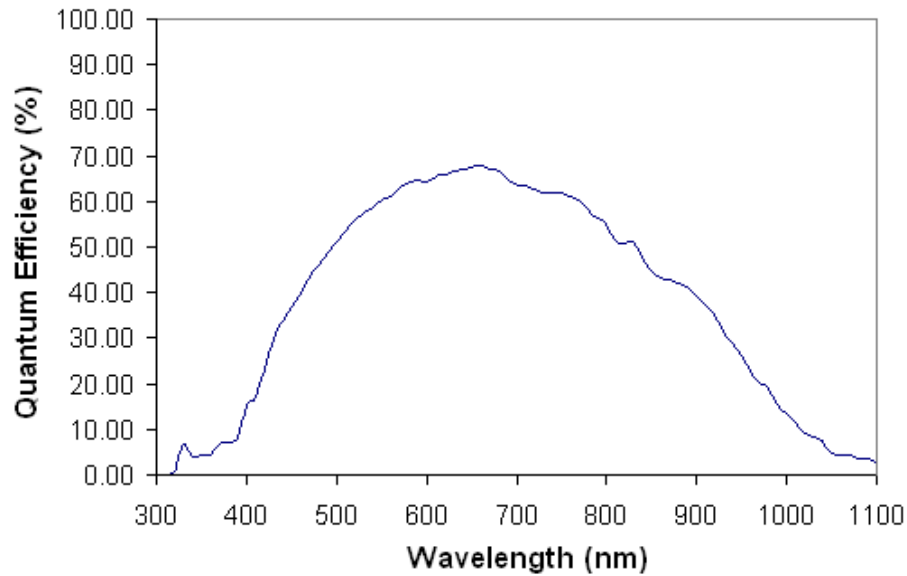


Figure 6.3. Spectral response of 6'' \times 6'' array of spherical diodes

6.3.2 Spectral Response of Low temperature Epitaxial Deposited Emitter

Instead of diffused emitter, the focus of this study is to investigate the feasibility of deposited emitter. However, the deposited emitter spherical diode is still in the stage of testing thus complete module is not yet ready for comprehensive measurement. A temporary prototype as shown in Figure 4.2 is set up for the spectral response measurement. The simple structure involves five spheres bonded on an aluminum disk with emitter layer and metal contact deposited on top of each sphere. The metal contact, which is aluminum, it is not a transparent contact thus the light would be completely blocked in the area of contact. Unlike the complete module mentioned in 6.3.1, no anti-reflection coating is applied so photons can be reflected by highly reflective silicon surface. Also, no passivation layer is used after emitter deposition. In order to complete the circuitry for measurement, a probe tip is used to contact the top metal. The probe tip creates a shade which covers almost half of the sphere. The spot size of the beam coming from the source is much larger than the area of the sphere. As a result, large amount of photons cannot even reach the sphere, causing extremely low external quantum efficiency. Taking all these factors into account, the absolute values of measured quantum efficiency exaggeratedly underestimate the

actual response of the diode. For most of the deposited film spherical diodes with non-transparent metal contact, the measured peak quantum efficiency recorded by the system is less than 1%. This value by no mean represents the actual quantum efficiency of a single diode. A few correction factors should be incorporated to account for the non-optimal experimental setup.

Due to the measurement setup, only one single diode can be measured at a time. The beam size coming from the system is of elliptical shape with diameters of 7.5 mm and 1.5 mm. The sphere, which the diameter is approximately 1 mm, is much smaller than the beam size. It is estimated that the sphere only covers about 11% of the area of the photon flux.

With the light beam directly placed on top of the sphere, only the upper hemisphere is counted as the active area which can absorb photons. The effective area where the emitter layer covers the sphere however is less than that due to directional deposition. The thickness across the surface varies as well from non-uniform deposition rate at different angles. The deposition on the vertical side wall can be very thin that it is insufficient to create a depletion region underneath. For such reason, the effective area needs to be recalculated as follows.

$$A = \int_0^{2\pi} \int_0^\alpha r^2 \sin \theta d\theta d\phi \quad (6.5)$$

α , the angle deviated from the positive z-axis in spherical coordinate, defines the coverage of the emitter film. So far no straightforward methodology has been derived to measure film thickness on spherical surface thus reasonable estimation is required. α of 60° is used because the thickness is assumed to be very thin beyond this angle and this assumption is likely to give less optimistic area coverage. Computing the integration gives an area of πr^2 .

Both the metal contact and the probe tip block part of the incoming flux from reaching the sphere. The metal contact is created by a shadow mask with openings of average diameter of 0.5 mm.

Assuming that the metal contact only covers the top of the sphere which is approximately flat, the area covered is estimated to be 0.2 mm^2 . It is very probable that under mask deposition occurs during the sputtering but the deposited area under the mask is relatively small compared to the size of the opening so the area mentioned above should be a valid approximation. The probe tip, which its diameter varies for different part of the tip, creates a shadow with significant size over the sphere. The actual shading area can be difficult to judge because of the presence of various uncertainties. The position, the angle and the size of the tip would affect the actual area covered. In addition, the tip covers part of the metal as well therefore the effect of light blocking from metal and probe tip should be considered as one factor. By metal contact itself, 16% of the area is covered. With the tip, as much as 30% of area is shaded estimated by crude visual judgment. To account for both effects, 35% shading area is assumed.

The finished module with diffused junction has an anti-reflection coating to minimize the reflection. This luxury is not presented in the prototype of deposited junction therefore significant amount of light is reflected since the reflectance of silicon is very high. The measurement of external quantum efficiency only counts the non-reflected photons thus presenting the prototype in a disadvantage. Without anti-reflection coating, the internal quantum efficiency should be used as a fair comparison and it is extracted by external quantum efficiency divided by $(1 - \text{Reflectance})$. To account for the reflection, the reflectance of the silicon should be analyzed. From Figure 6.4 (a), it is shown that for photons with wavelength of 500 nm or smaller, the refractive index is high in both real component and imaginary part [50]. For lower energy photons, the refractive index settles to a value of 3.5 with insignificant imaginary component. To calculate the reflected power the following formula is used.

$$P_r = \left(\frac{n_1 - n_2}{n_1 + n_2} \right)^2 \quad (6.6)$$

However, the sphere surface is not flat and Fresnel's equation should be used instead [51]. Due to the complexity in calculation and unknown polarization of beam, the spatial analysis of the sphere surface is discarded. From Figure 6.4 (b), the reflected power is higher for shorter wavelength as expected. For wavelength above 600 nm, less than one-third of the power is reflected. By inspecting the quantum efficiency spectrum shown in Figure 6.3, it is concluded that the efficiency of high energy photons is very small so the correction factor for reflection does not play a significant role in that region. For longer wavelength above 500 nm, the reflectance begins to settle to a value of 0.33. To simplify the calculation, a constant reflectance of 0.33 is applied to the whole spectrum.

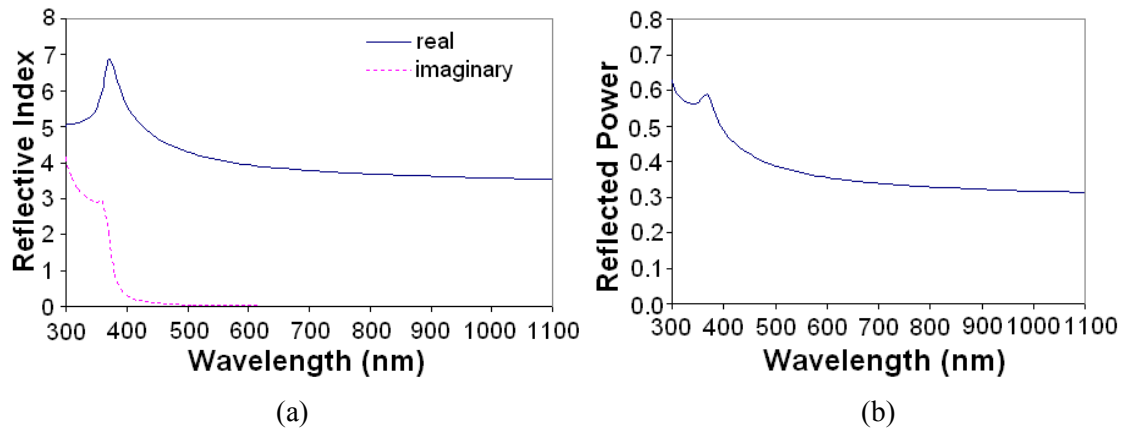


Figure 6.4 (a) The refractive index of silicon with real and imaginary component. (b) The reflected power calculated from the refractive index presented in (a) with Equation (6.6)

Incorporating all the factors mentioned above as listed in Table 6.1, the spectral response is scaled but the overall shape of the spectrum remains the same. The peak efficiency, originally at 0.4%, increases to 8.2%, which is 20 times larger than the measured value. The new estimate value of 8.2% is still much lower compared to the diffused junction at 68%. Other factors which have not been considered include low quality bulk, high surface recombination without passivation layer, and large recombination in the metal-silicon interface.

Table 6.1. Summary of correction factors in quantum efficiency measurement

Factors	Value
Coverage of beam size area	11%
Shading from tips and metal contact	35%
Reflection from silicon surface	33%

In the low temperature deposited emitter, the collection of high energy photons is not as efficient as the diffused junction. It is understandable due to the difference in junction quality. For diffused emitter diode, the junction is homogeneous with single crystalline structure. In deposited film diode, the junction is classified as heterogeneous as the low temperature epitaxial film possesses properties different from crystalline silicon. First of all, low temperature epitaxial film is not completely crystalline. Therefore the mismatch at the interface may cause the presence of defect states which increases the chance of recombination in the depletion layer. Looking at the normalized curve in Figure 6.5, the quantum efficiency for short wavelength photons is inferior in deposited junction compared to the diffused junction. For shallow junction, the high energy photons are more likely to be absorbed in the bulk and the efficiency should increase due to higher carrier lifetime in the bulk compared to emitter. The spectrometer measurement does not coincide with this conclusion. Both lower junction quality and high surface recombination rate in the deposited junction diode can result in lower quantum efficiency. With interface trap states at the junction, carriers reaching the junction are likely to recombine. In addition, the unpassivated layer having very high surface recombination rate in the range of 10^6 cm/s causes the carriers near the surface to recombine. The quantum efficiency at long wavelength is also lower for the prototype sphere because the bulk is classified as low quality for having short carrier lifetime. The finished module, made of high quality spheres, gives high collection efficiency for long wavelength photons absorbed in the bulk. It is also observed that the peak efficiency is blue shifted in deposited junction. In summary, deposited emitter can not match the performance of diffused emitter but it has the potential to be further developed for low cost photovoltaic application.

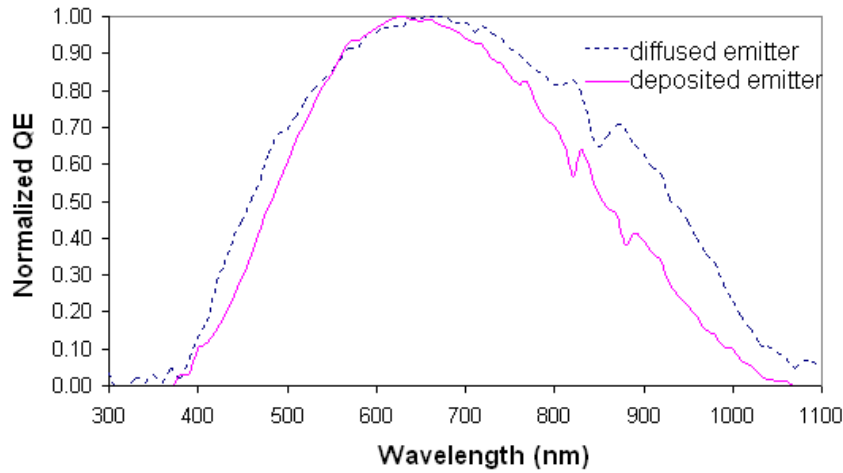


Figure 6.5. Normalized quantum efficiency of diffused emitter and low temperature epitaxial emitter on spheres

6.3.3 Effect of Emitter Thickness

The low temperature epitaxial emitter film with the following process parameters, 92% dilution, pressure of 200 mTorr and power of 90 W, is selected to study the effect of film thickness. From Figure 6.6, a few comments can be made. The film with 10 minutes of deposition, resulting in the lowest film thickness, is relatively effective in collecting the photons with higher energy. This observation can be explained by more short-wavelength photons being absorbed in the bulk due to shallower junction. The carriers generated in the bulk are more likely to diffuse to the space charge region due to higher bulk carrier lifetime. The carriers generated in the emitter film suffer from low lifetime because the heavily doped film is subjected to Auger recombination in addition. Theoretically, the film with 12 minutes deposition should have higher quantum efficiency in shorter wavelength photons compared to 15 minutes deposition but this result is not observed. For lower energy photons, thicker n⁺ emitter film gives better collection efficiency seen from the graph. Higher efficiency at longer wavelength suggests that the carrier lifetime in the bulk is better and/or the surface recombination is lower. However, the bulk characteristic should be the same in all cases. This observation may due to some secondary effects which are unknown in this stage. Also, a blue shift of the peak efficiency is observed when the thickness of the emitter layer is reduced.

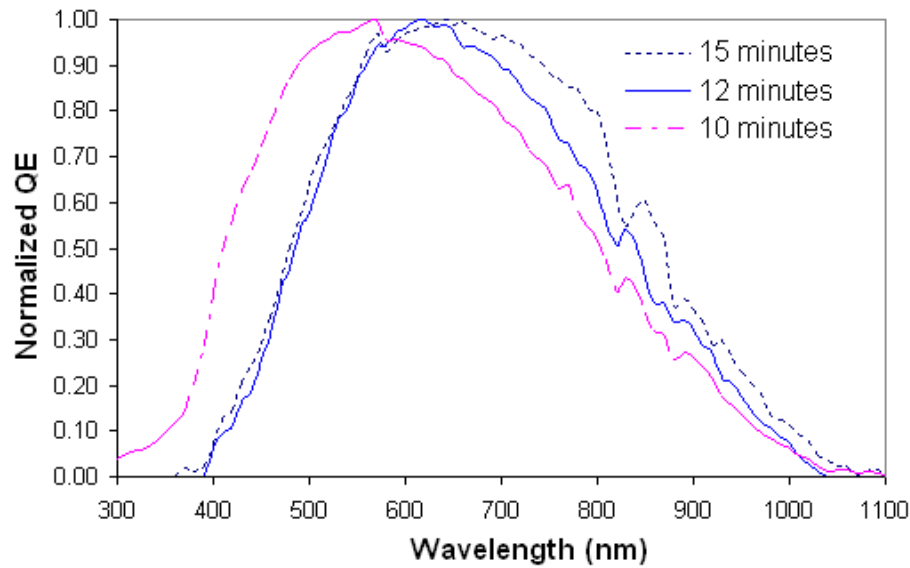


Figure 6.6. Normalized quantum efficiency of low temperature epitaxial emitter film deposited on sphere with 200 mTorr, 90W and varying deposition time

6.3.4 Effect of Transparent Conductive Oxide

In previous studies, the metal contact which is aluminum blocks significant part of diode area.

The use of transparent conductive oxide (TCO) can allow more light to enter the cell while giving a good contact for carrier collection. Instead of sputtering metal contact, a layer of indium oxide is deposited after emitter layer deposition. The indium oxide deposition is completed by reactive ion beam assisted evaporation (IBAE) with a thickness of 70 nm. This TCO has been proven to be a good conductor with resistivity in the range of $10^{-2} \Omega\text{-cm}$ and have a transmittance of 80% for photons with wavelength greater than 400 nm [52]. The use of TCO has raised the quantum efficiency to 4.8%, which is 10 times better than 0.4% with metal contact. It is implied that indium oxide can form a good contact with the emitter layer for efficient carrier collection. From the normalized quantum efficiency in Figure 6.7, contact with indium oxide performs better than aluminum in the high energy photon regime but appears worse in the low energy photon regime. The whole spectrum appears to be blue shifted with a narrower peak. Even though the spectrum is narrower than the one with aluminum, the impressive improvement from indium oxide encourages the use of transparent contact. To estimate the actual external quantum efficiency from the

TCO-deposited sample, the correction factors mentioned in 6.2.2 should be applied. With just the correction factor from beam size, the peak efficiency multiples 9 times, reaching 43%. Taking the shading effect into account, the peak efficiency can easily surpass 60%, approaching the peak efficiency of the module.

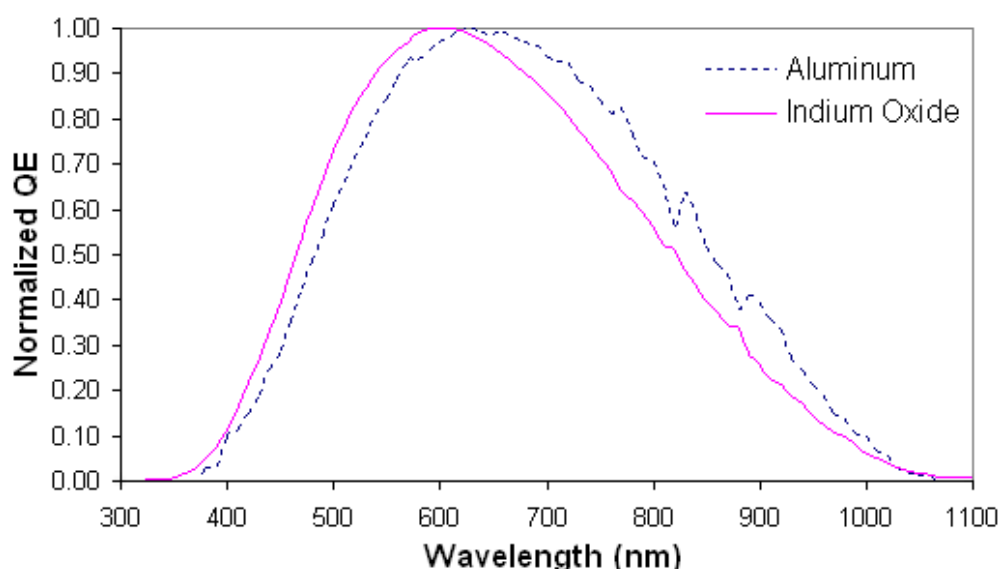


Figure 6.7. Normalized quantum efficiency of low temperature epitaxial emitter film deposited on sphere with aluminum contact and with indium oxide

6.3.5 Effect of Silicon Nitride as Insulation

Silicon nitride has some adverse effects on the quantum efficiency. As shown in Figure 6.8, the original efficiency of 0.4% without insulation is further degraded to 0.25%. In section 5 where the current-voltage characteristic is discussed, the current is in general lower with nitride as insulation because nitride was not completely removed from the surface forming a metal-insulator-semiconductor (MIS) junction. This poses a barrier for the minority carriers to be efficiently swept across the junction. The shape of the spectrum is not altered. The nitride should have a passivation effect of the bulk but no improvement of quantum efficiency in low energy photons is observed. The low quality bulk may have dominating effect over surface recombination.

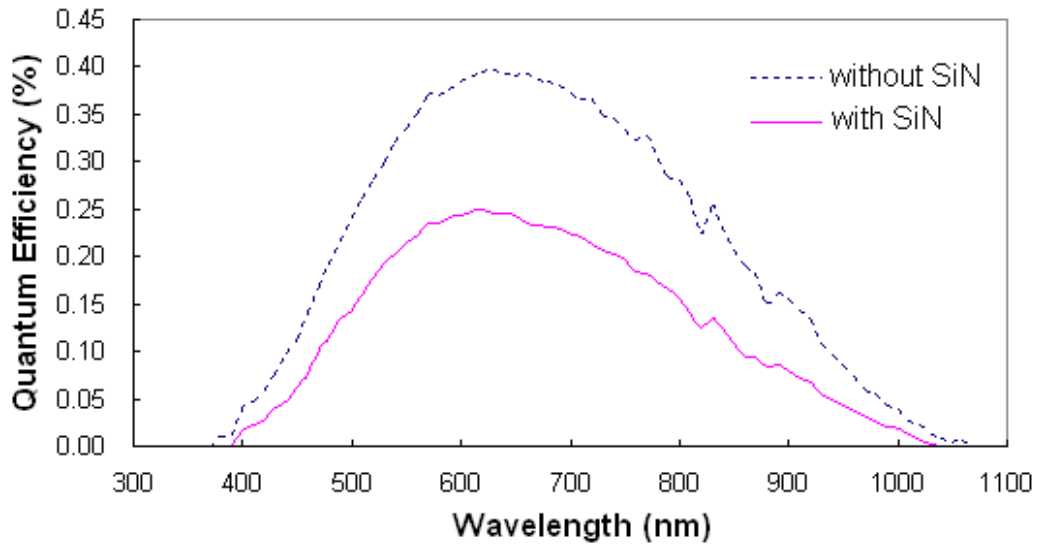


Figure 6.8. Quantum efficiency of low temperature epitaxial emitter film deposited on sphere with and without nitride as insulation layer

6.4 Summary

The low temperature epitaxial film on sphere does not show a significant response in the illuminated current-voltage measurement. It can be due to the fact that the device has not been fully optimized to give high short circuit current. Open circuit voltage, which is closely related to short circuit current, is observed to be extremely low as a result. Spectral response of spherical diode demonstrates that the diode can indeed collect photogenerated carriers but the magnitude of quantum efficiency is unreasonably low. The setup of the experiment only allows the individual sphere to intercept a fraction of the incoming photon flux. Using transparent conductive oxide instead of aluminum contact, making side contact pad, using high quality crystalline spheres and applying surface passivation are a few steps that should be taken in order to appropriately characterize the photovoltaic cell. With all the correction factors taken into account, the interpreted quantum efficiency would give a more reasonable value.

Chapter 7

Conclusions

In this thesis, two aspects of spherical solar cell have been studied. In material characterization, the charge kinetic in sphere is deduced from mathematical manipulation of the continuity equation. The overall photoconductivity decay response is mainly composed of the contributions from zeroth order fundamental decay mode and first order fundamental decay mode. Higher decay modes fade out quickly and their decay coefficients are small compared to the fundamental mode thus they do not have major contributions on the decay response.

Using microwave photoconductivity decay measurement, the effectiveness of rapid thermal oxide as surface passivation for silicon sphere is examined. The silicon dioxide growth by rapid thermal processing, with nitrogen anneal and controlled cooling, shows good passivation quality. The high temperature oxide growth however can degrade or improve the quality of the bulk depending on the initial quality of the sphere. This passivation technique can still be proven to be useful because surface recombination is a severe limitation in shallow emitter junction.

A low temperature deposited junction is reported for the first time. This low temperature step replaces high temperature diffusion process in traditional technology and eliminates emitter thinning process. A new set of process flow for device fabrication has been developed for spherical geometry since some of the techniques developed for the planar technology are not applicable to the new device structure. In this thesis, a spherical device without insulating layer has been developed to simplify the fabrication process. Experiments have been conducted to optimize the deposition parameters. Current-voltage measurement is used to characterize the junction quality. From the experimental results, this device gives a working diode characteristic although high reverse current is observed. The high reverse current implies that leakage current

paths exist between the emitter and the substrate. A silicon nitride layer is thus developed and applied to the spherical device. The insulating layer displays some improvement in reducing the reverse current but the reverse current level is still high compared to the planar counterpart. Comparing the current-voltage characteristic with planar wafer, the same deposited film exhibits inferior performance in the spherical diode. From the capacitance-voltage characteristic, it is concluded that the deposited junction is likely to be amorphous. This amorphous junction may cause the poor performance in spherical diode.

The illuminated current-voltage characteristic presents extremely low short circuit current. This short circuit current detrimentally impacts the open circuit voltage as well. The low short circuit current is a result of low external quantum efficiency. The low quantum efficiency is partly caused by the set up of the experiment because the sample is not optimized for the measurement. The application of transparent conductive oxide gives much higher quantum efficiency. Along with applicable correction factors, the quantum efficiency can be very well comparable to that of diffused emitter spherical module.

In this thesis, a working diode can be obtained from low temperature epitaxial film as emitter layer on silicon sphere. The performance of the diode is worse compared to the planar diode. The capacitance measurement suggests that the low temperature film is indeed amorphous. A set of extra treatments should be carried out to optimize the diode for proper characterization. High quality sphere should be used to decouple the recombination at the junction and the recombination in the bulk. Proper passivation must be applied to both the bulk and emitter to suppress surface recombination. Anti-reflective coating is recommended to reduce reflection from the sphere surface. Metal contact pad and probe tip should not cover the emitter layer. The spheres under test should be packed as close as possible to capture most of the photons. With all the optimizations techniques, a better illuminated diode characteristic should be observed.

References

- [1] H. Grabl, J. Kokott, M. Kulesa, J. Luther, F. Nuscheler, R. Sauerborn, H. J. Schellnhuber, R. Schubert, E. E. Schulze. “World in Transition Towards Sustainable Energy Systems”. German Advisory Council on Global Change. Earthscan, London. 2003.
- [2] M. A. Green. *Third Generation Photovoltaics: Advanced Solar Energy Conversion*. Springer Berlin Heidelberg. 2006.
- [3] A. Goetzberger, V. U. Hoffmann. “Photovoltaic Solar Energy Generation”. Springer-Verlag Berlin Heidelberg. New York. 2005.
- [4] W. R. McKee. “Development of the Spherical Silicon Solar Cell”. IEEE transactions on components, hybrids, and manufacturing technology, Vol. CHMT-5, No. 4, 1982. P. 366 – 341.
- [5] R. R. Schmit, M. D. Hammerbacher et al. “A Review of Spheral Solar Technology,” *Advances in Solar Energy*, Vol.10, 1995. P.347 – 379.
- [6] T. Minemoto, Y. Akashi, C. Okamoto, S. Omae, Y. Yamaguchi, M. Murozono, H. Takakura and Y. Hamakawa. “Spherical silicon solar cells fabricated by high speed dropping method”. 31st IEEE Photovoltaic Specialists Conference, 2005. P. 963 – 966.
- [7] J. D. Levine, D. K. Woodall, V. E. Knepprath and G. D. Stevens. “Upgrading of silicon spheres using an airjet grinder”. 23rd IEEE Photovoltaic Specialists Conference, 1993. P.201 – 204.
- [8] J. D. Levine, G. B. Hotchkiss and M. D. Hammerbacher. “Basic properties of the Spheral SolarTM Cell”. 22nd IEEE Photovoltaic Specialists Conference, Vol. 2, 1991. P. 1045 – 1048.
- [9] J. D. Plummer, M. D. Deal, P. B. Griffin. *Silicon VLSI Technology: Fundamentals, Practice and Modelling*. Prentice Hall. New Jersey. 2000.
- [10] O. Vetterl, F. Finger, R. Carius, P. Hapke, L. Houben, O. Kluth, A. Lambertz, A. Muck, B. Rech, H. Wagner. “Intrinsic microcrystalline silicon: A new material for photovoltaics”. *Solar Energy Materials and Solar Cells*, Vol. 62, 2000. P. 97 – 108.

- [11] A. V. Shah, J. Meier, E. Vallat-Sauvain, N. Wyrsh, U. Kroll, C. Droz, U. Graf. “Material and solar cell research in microcrystalline silicon”. *Solar Energy Materials and Solar Cells*, Vol 78, 2003. P. 469 – 491.
- [12] S. Hazra, S. Ray. “Nanocrystalline silicon as intrinsic layer in thin film solar cells”. *Solid State Communications*, Vol 109, 1999. P. 125 – 128.
- [13] D. K. Schroder. “Carrier Lifetimes in Silicon”. *IEEE Transactions on Electron Devices*. Vol 44, No. 1, 1997. P. 160 – 170.
- [14] M. J. Kerr and A. Cuevas. “General parameterization of Auger recombination in crystalline silicon”. *Journal of Applied Physics*, Vol 91, No. 4. 2002.
- [15] D. K. Schroder. *Semiconductor Material and Device Characterization*. Third Edition. John Wiley & Sons, Inc. 2006.
- [16] R. K. Ahrenkiel and S. Johnston. “Contactless Measurement of Recombination Lifetime in Photovoltaic Materials”. 26th IEEE Photovoltaic Specialists Conference, 1997. P. 119 – 122.
- [17] V. Grivickas, J. A. Tellefsen and M. Willander. “Surface recombination velocity in c-Si”. *Properties of Crystalline Silicon*. INSPEC. 1998.
- [18] M. Gharghi, G. Stevens, S. Sivoththaman. “Interpretation of Photo-conductivity Decay Lifetime in Silicon Sphere”. 4th IEEE World Conference on Photovoltaic Energy Conversion, 2006. P. 1138 – 1141.
- [19] Y. Ogita. “Bulk lifetime and surface recombination velocity measurement method in semiconductor wafers”. *Journal of Applied Physics*, Vol. 79, No. 9, 1996. P. 6954 – 6961.
- [20] J. K. Arch, J. S. Reynolds, M. D. Hammerbacher. “Characterization of Silicon Spheres for Spherical SolarTM Cell”. 24th IEEE Photovoltaic Energy Conversion, 2004. P. 1364 – 1367.
- [21] R.K. Ahrehkiel, D. Levi, J. Arch. “Recombination lifetime studies of silicon spheres”. *Solar Energy Materials and Solar Cells*, Vol 41/42, 1996. P. 171 – 181.
- [22] P. Doshi, J. Moschner, J. Jeong, A. Rohatgi, R. Singh, S. Narayanan. “Characterization and application of rapid thermal oxide surface passivation for the highest efficiency RTP silicon solar cells”. 26th IEEE Photovoltaic Specialists Conference, 1997. P. 87 – 90.

- [23] S. Sivoththaman, W. Laureys, P. D. Schepper, J. Nijs and R. Mertens. “Selective Emitters in Si by Single Step Rapid Thermal Diffusion for Photovoltaic Devices”. IEEE Electron Device Letters, Vol. 21, No. 6. 2000. P. 274 – 276.
- [24] S. G. dos Santos Filho, C. M. Hasenack, M. C. V. Lopes and V. Baranauskas. “Rapid thermal oxidation of silicon with different thermal annealing cycles in nitrogen: influence on surface microroughness and electrical characteristics”. Semiconductor Science and Technology, Vol. 10, 1995. P. 990 – 996.
- [25] O. Schultz, S. Riepe, S. W. Glunz. “Thermal degradation and gettering of solar grade multicrystalline silicon”. 19th European Photovoltaic Solar Energy Conference, 2004. P. 516 – 519.
- [26] S. Peters, J. Y. Lee, C. Ballif, D. Borchert, S. W. Gluz, W. Warta, and G. Willeke. “Rapid thermal processing: a comprehensive classification of silicon materials”. 29th IEEE Photovoltaic Specialists Conference, 2002. P. 214 – 217.
- [27] S. W. Glunz, J. Y. Lee, S. Rein. “Strategies for improving the efficiency of Cz-silicon solar cells”. 28th IEEE Photovoltaic Specialist Conference, 2000. P. 201 – 204.
- [28] T. Minemoto, C. Okamoto, S. Omae, M. Murozono, H. Takakura and Y. Hamakawa. “Fabrication of Spherical Silicon Solar Cells with Semi-Light-Concentration System”. Japanese Journal of Applied Physics, Vol. 44, No. 7A, 2005. P. 4820 – 4824.
- [29] M. Gharghi, “Spherical Silicon for Photovoltaic Applications: Material, Modeling and Devices”. University of Waterloo, PhD Thesis. 2007.
- [30] E. Conrad, K. V. Maydell, H. Angermann, C. Schubert and M. Schmidt. “Optimization of Interface Properties in a-Si:H/c-Si Heterojunction Solar Cells”. 4th World Conference on Photovoltaic Energy Conversion, Vol 2, 2006. P. 1263 – 1266.
- [31] F. Duerinckx, J. Szlufcik. “Defect passivation of industrial multicrystalline solar cells based on PECVD silicon nitride”. Solar Energy Materials and Solar Cells, Vol 72, Issue 1-4, 2002. P. 231 – 246.

- [32] M. Farrokh Baroughi and S. Sivoththaman. "A Novel Silicon Photovoltaic Cell Using a Low-Temperature Quasi-Epitaxial Silicon Emitter". IEEE Electron Device Letters, Vol 28, No. 7, 2007. P. 575 – 577.
- [33] A. C. Madayag and Z. Zhou. "Optimization of Spin-on-glass process for multilevel metalinterconnects". University/Government/Industry Microelectronics Symposium, 2001. Proceedings of the Fourteenth Biennial Volume, 2001. P. 136 – 139.
- [34] A. C. Madayag, Z. Zhou. "Optimization of spin-on-glass process for multilevel metal interconnects". University/Government/Industry Microelectronics Symposium, 2001. P. 136 – 139.
- [35] J. Schmidt, M. Kerr. "Highest-quality surface passivation of low-resistivity p-type silicon using stoichiometric PECVD silicon nitride". Solar Energy Materials and Solar Cells, Vol. 65, 2001. P. 585 – 591.
- [36] E. Radziemska. "Dark I-U-T measurements of single crystalline silicon solar cells". Energy conversion and Management, Vol. 46, 2005. P. 1485 – 1494.
- [37] S. S. Han, M. Ceiler, S. A. Bidstrup, P. Kohn and G. May. "Modeling the Properties of PECVD Silicon Dioxide Films Using Optimized Back-Propagation Neural Networks". IEEE transactions on components, packaging, and manufacturing technology – part A, Vol 17, No. 2, 1994. P. 174 – 182.
- [38] S. Mukhopadhyay, D. Das, and S. Ray. "Better control over the onset of microcrystallinity in fast-growing silicon network". Journal of Material Research, Vol. 19, No. 9, 2004. P. 2597 – 2603.
- [39] M. Farrokh Baroughi and S. Sivoththaman. "A Novel Si-Based Heterojunction Solar Cell without Transparent Conductive Oxide". 4th World Conference on Photovoltaic Energy Conversion, Vol. 1, 2006. P. 83 – 86.
- [40] P. N. Murgatrody. "Theory of space-charged-limited current enhanced by Frenkel effect". Journal of Applied Physics D, Vol 3, 1970. P. 151 – 156.
- [41] K. Lips, W. Fuhs, and F. Fingers. "Recombination currents in microcrystalline silicon solar cells studied by electrically detected magnetic resonance". 29th IEEE Photovoltaic Specialists Conference, 2002. P. 1166 – 1169.

- [42] M. El-Tahchi, A. Khoury, M. D. Labardonnée, P. Mialhe, F. Pelanchon. “Degradation of the diode ideality factor of silicon n-p junctions”, *Solar Energy Materials and Solar Cells*, Vol. 62, 2000. P. 393 – 398.
- [43] B. G. Streetman, S. Banerjee. “Solid State Electronic Devices”. Fifth Edition. Prentice Hall. New Jersey. 2000.
- [44] M. Farrokh Baroughi, R. Jeyakumar, Y. Vygranenko, F. Khalvati, S. Sivoththaman. “Fabrication and characterization of amorphous Si/crystalline Si heterojunction devices for photovoltaic applications”. *Journal of Vacuum Science Technology*, Vol. A 22, Issue 3, 2004. P. 1015 – 1019.
- [45] R. A. Street. *Hydrogenated Amorphous Silicon*. Cambridge University Press. United Kingdom. 1991.
- [46] T. H. Wang, E. Iwaniczko, M. R. Page, D. H. Levi, Y. Yan, H. M. Branz, Q. Wang, V. Yelundur and A. Rohatgi. “Effective Interfaces in Silicon Heterojunction Solar Cells”. 31st IEEE Photovoltaics Specialist Conference and Exhibition, 2005. P. 955 – 958.
- [47] H. Matsuura. “Hydrogenated Amorphous-Silicon/Crystalline-Silicon Heterojunctions : Properties and Applications”. *IEEE Transactions on Electron Devices*, Vol 36, No. 12, 1989. P. 2908 – 2914.
- [48] “Dolan-Jenner Fiber Optic Illuminators”. Terran Technology, Inc; Labtek Division. 1998. <http://www.labtek.net/Dolan-Jenner.htm> [Access: July 30, 2008]
- [49] J. Nelson. *The Physics of Solar Cells*. Imperial College Press. London. 2003.
- [50] Green and Keevers. “Optical properties of silicon”. <http://www.udel.edu/igert/pvcdrom/APPEND/OPTICAL.HTM> [Access: July 24, 2008]
- [51] A. Haapalinna, P. Kärhä, and E. Ikonen. “Spectral Reflectance of Silicon Photodiodes”. *Applied Optics*, Vol 37, 1998. P. 729 – 732.
- [52] K. Wang. “Transparent Oxide Semiconductors: Fabrication, Properties, and Applications”. University of Waterloo, PhD Thesis. 2008.

Appendix A

Calculation of Conductivity Decay Coefficients

The solution of Δn and initial conditions are

$$\Delta n(r, \theta) = \sum_m \sum_i \Gamma_{m,i} \exp \left[- \left(\frac{1}{\tau_b} + D \frac{\lambda_{m,i}^2}{R^2} \right) t \right] j_m \left(\lambda_{m,i} \frac{r}{R} \right) P_m(\cos \theta) \quad (\text{A.1})$$

$$\Delta n(r, \theta, 0) = g_0 \frac{1}{r^2} \cos \theta \exp(-\alpha(R-r)) \quad (\text{for upper hemisphere}) \quad (\text{A.2})$$

$$\Delta n(r, \theta, 0) = g_0 \frac{1}{r^2} \cos(\pi - \theta) \exp(-\alpha(R+r)) \quad (\text{for lower hemisphere}) \quad (\text{A.3})$$

Using the way to find the coefficients in fourier series, the following expression can be integrated on both side to get $\Gamma_{m,i}$. The orthogonality of the spherical Bessel and Legendre functions only allow the terms $m = n$ to exist.

$$j_n(\lambda_{n,j} \frac{r}{R}) P_n(\cos \theta) \Delta n(r, \theta, 0) = \sum_{j=0} \sum_{n=0} \Gamma_{m,i} j_m(\lambda_{m,i} \frac{r}{R}) P_m(\cos \theta) j_n(\lambda_{n,j} \frac{r}{R}) P_n(\cos \theta) \quad (\text{A.4})$$

For $0 \leq \theta \leq \pi/2$ (upper hemisphere),

$$\begin{aligned} \Gamma_{m,i,u} &= \frac{g_0 \int_0^{\pi/2} \int_0^R \frac{1}{r^2} j_m(\lambda_{m,i} \frac{r}{R}) P_m(\cos \theta) \cos \theta e^{-\alpha(R-r)} r^2 \sin \theta dr d\theta}{\int_0^R j_m^2(\lambda_{m,i} \frac{r}{R}) r^2 dr \int_0^{\pi} P_m^2(\cos \theta) \sin \theta d\theta} \\ &= \frac{g_0 \int_0^R \frac{1}{r^2} j_m(\lambda_{m,i} \frac{r}{R}) e^{-\alpha(R-r)} r^2 dr \int_0^{\pi/2} P_m(\cos \theta) \cos \theta \sin \theta d\theta}{\int_0^R j_m^2(\lambda_{m,i} \frac{r}{R}) r^2 dr \int_0^{\pi} P_m^2(\cos \theta) \sin \theta d\theta} \end{aligned} \quad (\text{A.5})$$

For $\pi/2 \leq \theta \leq \pi$ (lower hemisphere),

$$\Gamma_{m,i,l} = \frac{g_0 \int_{\pi/2}^{\pi} \int_0^R \frac{1}{r^2} j_m(\lambda_{m,i} \frac{r}{R}) P_m(\cos \theta) \cos(\pi - \theta) e^{-\alpha(R+r)} r^2 \sin \theta dr d\theta}{\int_0^R j_m^2(\lambda_{m,i} \frac{r}{R}) r^2 dr \int_0^{\pi} P_m^2(\cos \theta) \sin \theta d\theta}$$

$$= \frac{g_0 \int_0^R \frac{1}{r^2} j_m(\lambda_{m,i} \frac{r}{R}) e^{-\alpha(R+r)} r^2 dr \int_{\pi/2}^{\pi} P_m(\cos \theta) \cos(\pi - \theta) \sin \theta d\theta}{\int_0^R j_m^2(\lambda_{m,i} \frac{r}{R}) r^2 dr \int_0^{\pi/2} P_m^2(\cos \theta) \sin \theta d\theta} \quad (\text{A.6})$$

Looking at the second term representing the lower hemisphere contribution, let $\Psi'_{m,i,l}$ and $\Gamma'_{m,i,l}$ be the coefficients depending on r only, keeping θ fixed.

$$\Psi'_{m,i,l} = \Gamma'_{m,i,l} \int_0^R j_m(\lambda_{m,i} \frac{r}{R}) r^2 dr = g_0 \left(\frac{\int_0^R \frac{1}{r^2} j_m(\lambda_{m,i} \frac{r}{R}) e^{-\alpha(R+r)} r^2 dr}{\int_0^R j_m^2(\lambda_{m,i} \frac{r}{R}) r^2 dr} \right) \int_0^R j_m(\lambda_{m,i} \frac{r}{R}) r^2 dr \quad (\text{A.7})$$

The integral in the numerator of $\Gamma'_{m,i,l}$ turns out to be very small because the radius (0.04 cm) is an order of magnitude larger than absorption depth (0.0032 cm). Comparing this term to the one in the upper hemisphere, the numerical integration values in the lower hemisphere are three orders smaller. Therefore, it is safe to neglect any calculation in the lower hemisphere.

Focusing on the upper hemisphere, the expression can be simplified by inspecting the legendre function. Let $\Psi''_{m,i,u}$ and $\Gamma''_{m,i,u}$ be the coefficients depending on θ only, keeping r fixed.

$$\Psi''_{m,i,u} = \Gamma''_{m,i,u} \int_0^{\pi/2} P_m(\cos \theta) \sin \theta d\theta = g_0 \left(\frac{\int_0^{\pi/2} P_m(\cos \theta) \cos \theta \sin \theta d\theta}{\int_0^{\pi/2} P_m^2(\cos \theta) \sin \theta d\theta} \right) \int_0^{\pi/2} P_m(\cos \theta) \sin \theta d\theta \quad (\text{A.8})$$

It turns out that the integral in the numerator of $\Gamma''_{m,i,u}$ only has zeroth, first order and even orders.

The last integral in the numerator of $\Psi''_{m,i,u}$ on the other hand only has zeroth and odd orders.

Multiplying these two integrals together results in non-zero values for zeroth and first order, eliminating higher orders contribution. The resultant Ψ becomes

$$\Psi_{m,i} = \Gamma_{m,i} \int_0^R j_m(\lambda_{m,i} \frac{r}{R}) r^2 dr \int_0^{\pi/2} P_m(\cos \theta) \sin \theta d\theta \int_0^{2\pi} d\phi \quad m = 0, 1 \quad (\text{A.9})$$

The expression of gammas in (A.5) can be divided into two separate components, the spherical Bessel part and the Legendre part.

$$\Gamma_{m,i} = g_0 \left(\frac{\int_0^R \frac{1}{r^2} j_m(\lambda_{m,i} \frac{r}{R}) e^{-\alpha(R-r)} r^2 dr}{\int_0^R j_m^2(\lambda_{m,i} \frac{r}{R}) r^2 dr} \right) \left(\frac{\int_0^{\pi/2} P_m(\cos \theta) \cos \theta \sin \theta d\theta}{\int_0^{\pi} P_m^2(\cos \theta) \sin \theta d\theta} \right) \quad (\text{A.10})$$

The integration on the Legendre part is straightforward. The integration of the Bessel function however is not analytic thus numerical integration is performed. There is another complication with this integral. The zeroth order of the spherical Bessel function is

$$j_0(x) = \frac{\sin(x)}{x} = \text{sinc}(x) \quad (\text{A.11})$$

The sinc function has a maximum at 0 and its envelop decays with 1/x. The initial condition to be met is an exponential function having a maximum at the surface with $r = R$ and it decays exponentially. The set up of the whole problem defines that $r = 0$ is at the center. In that case, the integration of the spherical Bessel integral would not be able to give appropriate fourier series coefficients to approximate the exponential function. To solve this problem, the integral is revised so that $r = 0$ is at the surface.

$$\Gamma_{m,i,u} = g_0 \left(\frac{\int_0^R \frac{1}{(R-r)^2} j_m(\lambda_{m,i} \frac{r}{R}) e^{-\alpha r} r^2 dr}{\int_0^R j_m^2(\lambda_{m,i} \frac{r}{R}) r^2 dr} \right) \left(\frac{\int_0^{\pi/2} P_m(\cos \theta) \cos \theta \sin \theta d\theta}{\int_0^{\pi} P_m^2(\cos \theta) \sin \theta d\theta} \right) = g_0 \Gamma'_{m,i} \Gamma''_{m,i} \quad (\text{A.12})$$

where $\Gamma'_{m,i}$ represents the coefficient from the Bessel integral and $\Gamma''_{m,i}$ represents the coefficient from the Legendre. The integrations can then be carried out numerically for $\Gamma'_{m,i}$ and analytically for $\Gamma''_{m,i}$.

Appendix B

Conductivity Decay Coefficients

The following parameters are used to generate the values.

Diffusion Coefficient $D_n = 30 \text{ cm}^2/\text{s}$

Absorption Coefficient $\alpha = 312.5 \text{ cm}^{-1}$

Since the contribution of Γ'' and integration of ϕ is the same for all orders and mode, their value will not be listed in the table below.

Radius $R = 0.03 \text{ cm}$; Surface recombination velocity $S = 10 \text{ cm/s}$

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	0.1730	170.88	9.018×10^{-6}	1.541×10^{-3}	1.0
0, 2	4.4957	-310.35	-1.836×10^{-8}	5.699×10^{-6}	0.0
0, 3	7.7265	886.92	7.911×10^{-9}	7.016×10^{-6}	0.0
1, 1	2.0905	457.55	3.503×10^{-6}	1.603×10^{-3}	1.04
1, 2	5.9422	-461.60	2.649×10^{-7}	-1.223×10^{-4}	-0.08

Radius $R = 0.03 \text{ cm}$; Surface recombination velocity $S = 100 \text{ cm/s}$

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	0.5423	173.29	8.781×10^{-6}	1.522×10^{-3}	1.0
0, 2	4.5157	-312.47	-3.859×10^{-8}	1.206×10^{-5}	0.01
0, 3	7.7382	888.05	1.148×10^{-8}	1.020×10^{-5}	0.01
1, 1	2.1677	447.40	3.549×10^{-6}	1.588×10^{-3}	1.04
1, 2	5.9582	-464.04	2.488×10^{-7}	-1.155×10^{-4}	-0.08

Radius R = 0.03 cm; Surface recombination velocity S = 1000 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	1.5708	190.72	6.997×10^{-6}	1.334×10^{-3}	1.0
0, 2	4.5156	-329.65	-2.651×10^{-7}	8.738×10^{-5}	0.07
0, 3	7.7382	898.88	5.981×10^{-8}	5.376×10^{-5}	0.04
1, 1	2.1677	393.99	3.652×10^{-6}	1.439×10^{-3}	1.08
1, 2	5.9582	-477.64	1.152×10^{-7}	-5.500×10^{-5}	-0.04

Radius R = 0.03 cm; Surface recombination velocity S = 10000 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	2.8363	165.39	3.551×10^{-6}	5.874×10^{-4}	1.0
0, 2	5.7172	-181.89	-7.779×10^{-7}	1.417×10^{-4}	0.24
0, 3	8.6587	739.40	2.921×10^{-7}	2.160×10^{-4}	0.37
1, 1	4.0662	258.32	2.590×10^{-6}	6.691×10^{-4}	1.14
1, 2	7.0568	-300.99	-3.396×10^{-7}	1.022×10^{-4}	0.17

Radius R = 0.03 cm; Surface recombination velocity S = 100000 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	3.1102	119.41	2.819×10^{-6}	3.366×10^{-4}	1.0
0, 2	6.2204	51.280	-7.040×10^{-7}	-3.610×10^{-5}	-0.11
0, 3	9.3308	320.98	3.124×10^{-7}	1.000×10^{-4}	0.30
1, 1	4.4485	150.67	2.091×10^{-6}	3.151×10^{-4}	0.94
1, 2	7.6481	34.006	-3.562×10^{-7}	-1.211×10^{-5}	-0.04

Radius R = 0.03 cm; Surface recombination velocity S = 1000000 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	3.1385	112.63	2.740×10^{-6}	3.086×10^{-4}	1.0
0, 2	6.2769	87.293	-6.850×10^{-7}	-5.979×10^{-5}	-0.19
0, 3	9.4154	245.32	3.044×10^{-7}	7.468×10^{-5}	0.24
1, 1	4.4889	135.38	2.0344×10^{-6}	2.754×10^{-4}	0.89
1, 2	7.7175	85.281	-3.477×10^{-7}	-2.965×10^{-5}	-0.10

Radius R = 0.04 cm; Surface recombination velocity S = 10 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	0.1997	8.8768	2.133×10^{-5}	1.893×10^{-4}	1.0
0, 2	4.4964	20.515	-2.540×10^{-8}	-5.211×10^{-7}	0.0
0, 3	7.7270	80.491	1.532×10^{-8}	1.233×10^{-6}	0.01
1, 1	2.0934	19.160	8.296×10^{-6}	1.590×10^{-4}	0.84
1, 2	5.9427	9.8358	6.267×10^{-7}	6.164×10^{-6}	0.03

Radius R = 0.04 cm; Surface recombination velocity S = 100 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	0.6241	9.1888	2.059×10^{-5}	1.892×10^{-4}	1.0
0, 2	4.5231	20.456	-1.077×10^{-7}	-2.204×10^{-6}	-0.01
0, 3	7.7425	80.509	2.801×10^{-8}	2.255×10^{-6}	0.01
1, 1	2.1950	18.757	8.433×10^{-6}	1.582×10^{-4}	0.84
1, 2	5.9642	9.8191	5.816×10^{-7}	5.711×10^{-6}	0.03

Radius R = 0.04 cm; Surface recombination velocity S = 1000 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	1.7582	12.010	1.547×10^{-5}	1.858×10^{-4}	1.0
0, 2	4.7820	20.368	-7.952×10^{-7}	-1.620×10^{-5}	-0.09
0, 3	7.8962	80.419	1.831×10^{-7}	1.473×10^{-5}	0.08
1, 1	2.8966	17.550	8.556×10^{-6}	1.502×10^{-4}	0.81
1, 2	6.1737	10.088	1.731×10^{-7}	1.746×10^{-6}	0.01

Radius R = 0.04 cm; Surface recombination velocity S = 10000 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	2.9100	19.234	7.958×10^{-6}	1.531×10^{-4}	1.0
0, 2	5.8409	33.210	-1.839×10^{-6}	-6.107×10^{-5}	-0.40
0, 3	8.8048	72.637	7.306×10^{-7}	5.306×10^{-5}	0.35
1, 1	4.1664	18.504	5.847×10^{-6}	1.082×10^{-4}	0.71
1, 2	7.1954	24.547	-8.510×10^{-7}	-2.089×10^{-5}	-0.14

Radius R = 0.04 cm; Surface recombination velocity S = 100000 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	3.1180	20.769	6.619×10^{-6}	1.375×10^{-4}	1.0
0, 2	6.2361	44.782	-1.654×10^{-6}	-7.407×10^{-5}	-0.54
0, 3	9.3542	63.433	7.365×10^{-7}	4.672×10^{-5}	0.34
1, 1	4.4597	18.193	4.919×10^{-6}	8.949×10^{-5}	0.65
1, 2	7.6674	39.558	-8.383×10^{-7}	-3.316×10^{-5}	-0.24

Radius R = 0.04 cm; Surface recombination velocity S = 1000000 cm/s

m,i	λ	Γ'	Integral of Bessel	Ψ	Ψ normalized
0, 1	3.1392	20.904	6.494×10^{-6}	1.358×10^{-4}	1.0
0, 2	6.2785	46.112	-1.624×10^{-6}	-7.487×10^{-5}	-0.55
0, 3	9.4177	61.935	7.216×10^{-7}	4.469×10^{-5}	0.33
1, 1	4.4900	18.122	4.822×10^{-6}	8.739×10^{-5}	0.64
1, 2	7.7195	41.436	-8.232×10^{-7}	-3.411×10^{-5}	-0.25